GPS

locate, communicate, accelerate

UBX-G6010, UBX-G6000/UBX-G0010

u-blox 6 single chips and chipsets

Data Sheet

Abstract

Technical Data Sheet describing the UBX-G6010 and UBX-G6000/UBX-G0010 single chip and chipset GPS receivers. Featuring the high-performance u-blox 6 GPS position engine, the UBX-G6010 and UBX-G6000/UBX-G0010 require no external host and provide high sensitivity and fast acquisition/tracking times at low cost and power consumption.

Features include intelligent, user configurable power management, support for YUMA Capture & Process technology and support for u-blox' AssistNow Online and AssistNow Offline A-GPS services.

The UBX-G6010 and UBX-G6000/UBX-G0010 are available in 8x8 mm single-chip or 9x9 & 4x4 mm dual-chip packages.

Document Information	
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Document status information	
Objective Specification	This document contains target values. Revised and supplementary data will be published later.
Advance Information	This document contains data based on early testing. Revised and supplementary data will be published later.
Preliminary	This document contains data from product verification. Revised and supplementary data may be published later.
Released	This document contains the final product specification.

This document applies to the following products:

Name	Type number	ROM/FLASH version	PCN reference
UBX-G6010 Single package (Standard)	UBX-G6010-ST B0600 B	6.02	N/A
UBX-G6010 Single package (Automotive)	UBX-G6010-SA B0600 B	6.02	N/A
UBX-G6000 Baseband Processor (Automotive)	UBX-G6000-BA B0600	6.02	N/A
UBX-G0010 RF Front-End (Automotive)	UBX-G0010-QA B		N/A

Contents

1 Functional description

1.1 Overview

The UBX-G6010 and UBX-G6000/UBX-G0010 are the newest generation single chip and chipset GPS receivers from u-blox and demonstrate our continuing commitment to advancing GPS technology. Featuring the high performance u-blox-6 position engine, the UBX-G6010 and UBX-G6000/UBX-G0010 provide even better sensitivity and acquisition times while requiring no external host. Sophisticated RF-architecture and interference suppression ensure maximum performance even in GPS-hostile environments.

u-blox 6 technology has been designed with low power consumption and low costs in mind, and still delivers high performance GPS. Integrated Capture & Process[1] support and intelligent power management are breakthroughs for low-power applications. The minimal BOM requires as few as 19 passive components, an LDO and LNA are built in and costly external memory is not needed. Lower price GPS crystals as well as TCXOs are supported, and 2-layer PCB integration capability and small footprint ensure further cost savings. The UBX-G6010 is the ideal solution for cost sensitive applications that don't require firmware update capability, while the UBX-G6000/UBX-G0010 supports external memory where firmware update capability is required.

1.2 Highlights and features

Highlights

- u-blox 6 position engine with over 2 million effective correlators featuring < 1 s acquisition, –147 dBm coldstart acquisition sensitivity and 5 Hz update rate
- Supports ultra-low power logging and geo-tagging applications with Capture & Process (<0.2 s capture time)
- Intelligent, user configurable power management for radically lower power consumption
- Supports u-blox' AssistNow Online / AssistNow Offline A-GPS services and is OMA SUPL compliant
- GALILEO ready
- Automotive qualified
- Minimal BOM costs

Features

	Chip Size (mm)	TCXO	GPS Crystal	FW Update / FLASH	Power Save mode	UART	USB	SPI	DDC	Capture & Process	AssistNow Online	AssistNow Offline	Dead Reckoning	Raw Data	Precision Timing	Timepulse	CFG Pins	Reset Input	Antenna Supply	Antenna Supervisor
UBX-G6010	**8x8**	**O**	•		•	**1**	**1**	**1**	**1**	•	•	•				**2**	**10**	•	•	•
UBX-G6000 UBX-G0010	**9x9 4x4**	**O**	•	**F**	•	**2**	**1**	**1**	**1**	•	•	•				**2**	**12**	•	•	•

F = Requires external FLASH, O = Optional

Table 1: Features of UBX-G6010 and UBX-G6000/UBX-G0010

[1] Capture & Process is u-blox' patented technology featuring ultra-fast position capture and ultra-low power consumption. The separately available software product YUMA is required for implementation of Capture & Process technology.

1.3 GPS performance

Parameter	Specification		
Receiver type	50 Channels GPS L1 frequency, C/A Code GALILEO Open Service L1 frequency		
Time-To-First-Fix[2]		TCXO	Crystal
	Cold Start (Autonomous)	29 s	32 s
	Warm Start (Autonomous)	29 s	32 s
	Hot Start (Autonomous)	<1 s	<1 s
	Aided Starts[3]	<1 s	<3 s
	Capture Time (Capture & Process)	<0.2 s	<0.2 s
Sensitivity[4]		TCXO	Crystal
	Tracking & Navigation	-160 dBm	-160 dBm
	Reacquisition	-160 dBm	-160 dBm
	Cold Start (Autonomous)	-147 dBm	-146 dBm
Horizontal position accuracy[5]	Autonomous	< 2.5 m	
	SBAS	< 2.0 m	
Accuracy of Timepulse signal	RMS 99% Time Pulse	30 ns <60 ns Configurable f = 0.25 Hz … 1 kHz (Tp = 1/f = 4 s … 1 ms)	
Max navigation update rate		up to 5Hz (ROM) / 2Hz FLASH	
Velocity accuracy[6]		0.1m/s	
Heading accuracy[7]		0.5 degrees	
Dynamics		≤ 4 g	
Operational limits[8]	Altitude Velocity	50000 m 500 m/s	

Table 2: GPS performance

[2] All satellites at -130 dBm
[3] Dependent on aiding data connection speed and latency
[4] Demonstrated with a good active antenna
[5] CEP, 50%, 24 hours static, -130dBm, SEP: <3.5m
[6] 50% @ 30 m/s
[7] 50% @ 30 m/s
[8] Assuming Airborne <4g platform

1.4 Block diagrams

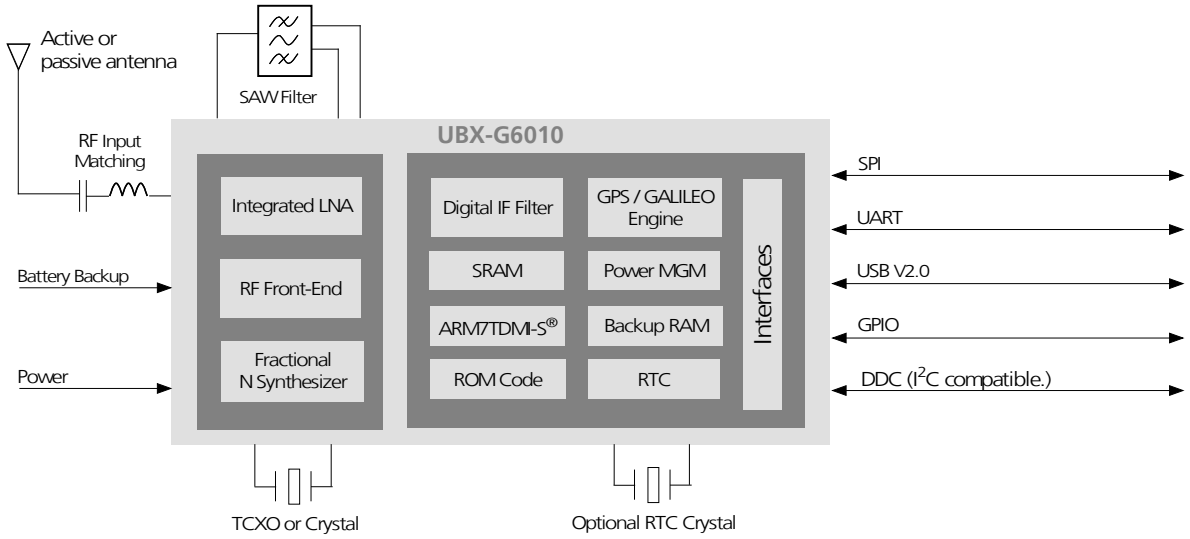


Figure 1: UBX-G6010 single-chip GPS receiver: block diagram

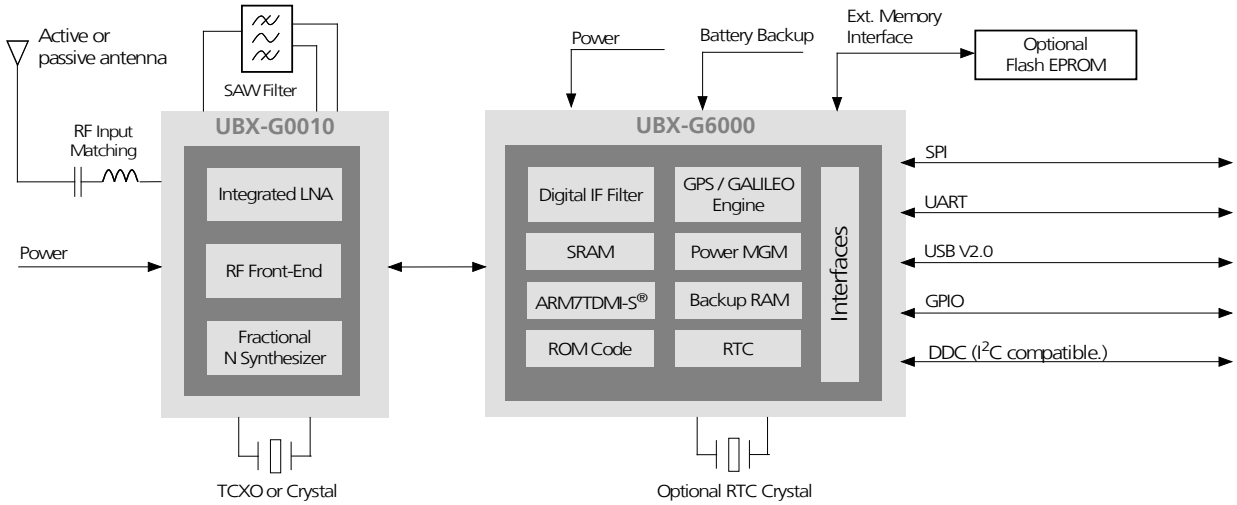


Figure 2: UBX-G0010 / UBX-G6000 dual-chip GPS receiver: block diagram

1.5 Assisted GPS (A-GPS)

Supply of aiding information like ephemeris, almanac, rough last position and time and satellite status and an optional time synchronization signal will reduce time to first fix significantly and improve the acquisition sensitivity. All u-blox 6 ICs support the u-blox AssistNow Online and AssistNow Offline A-GPS services and are OMA SUPL compliant.

1.6 SuperSense Indoor GPS

All u-blox 6 ICs come with SuperSense, providing ultra-fast acquisition/reacquisition and exceptional tracking sensitivity. SuperSense enables best-in-class tracking and navigation in difficult signal environments such as urban canyons or indoor locations.

1.7 KickStart / oscillators

A feature available with u-blox 6 is KickStart. This functionality uses a TCXO to accelerate weak signal acquisition, enabling faster start and reacquisition times.

1.8 GALILEO

u-blox 6 receivers receive and track GPS and GALILEO signals simultaneously, enhancing accuracy and coverage. When GALILEO-L1 signals become available, u-blox 6 receivers equipped with FLASH memory will be capable of receiving and processing them via a simple upgrade. The ability to receive and track GALILEO satellite signals will result in higher coverage, improved reliability and better accuracy.

1.9 Capture & Process software and service from u-blox

Capture & Process is a different way of calculating GPS position, where the location is not needed immediately, but somewhere later in time. The benefits of this technology lie in not needing to download the slowly transmitted satellite information data from GPS signal at the time of capture, but providing it at the user's convenience through an internet link to the processing software. This results in extremely short times (<0.2s) to create a snapshot of the GPS signal ("Capture") and thus very low power consumption. It also frees the user from having to wait until satellite information data is available.

Depending on the use-case, either realtime-GPS with standalone position calculation or Capture & Process with subsequent position calculation provide the greatest advantage to the user.

The two steps for Capture & Process are:

1. Capture: perform a single or multiple captures on a mobile device with a u-blox' GPS receiver, and transfer the data (typically 120 kByte per capture) to an application processor which can store it on a mass storage device.

2. Process: connect the storage device to a MAC or PC which is connected to the internet, and use u-blox' YUMA software to calculate position from the snapshot from the GPS receiver and the data provided by u-blox' online service.

YUMA is the software and service component of u-blox' Capture & Process technology. u-blox 6 features a powerful hardware to capture raw GPS signal data required by YUMA, and has very low demands on the application processor in terms of supported interfaces and their speed. Data transfer to the application processor is possible via UART, USB, SPI and DDC (I2C) interfaces.

YUMA is particularly useful for mobile logging and tracking applications where low power consumption is critical, and is a must for photo geotagging capability with cameras. Other applications include bike computers, waypoint loggers, asset/animal trackers, etc.

1.10 Protocols and interfaces

Protocol	Type
NMEA	Input/output, ASCII, 0183, 2.3 (compatible to 3.0)
UBX	Input/output, binary, u-blox proprietary

Table 3: Available Protocols

Both protocols are available on UART, USB, DDC and SPI. For specification of the various protocols see the *u-blox 5 & u-blox 6 Receiver Description Including Protocol Specification* [2].

1.11 Power management

u-blox 6 technology offers power optimized architecture with built-in autonomous power saving functions that minimize power consumption at any given time. The receiver can be operated in 2 different continuous operating modes: Maximum Performance, and Eco Mode. In addition an intermittent Power Save Mode allows reducing the average tracking current consumption by periodically switching off parts of or the complete GPS receiver and waking it up at configurable intervals. For more information, see *Chapter 4*

2 Digital IC and mixed-signal subsystem

The baseband-IC integrates an ARM7TDMI-S™ CPU and all the memory required for embedded firmware execution. Specific hardware required for signal acquisition and tracking and a wide selection of peripheral interfaces are provided. Analog functional blocks such as PLL, A/D converters and Power Management Unit (PMU) are fully integrated. u-blox 6's embedded firmware provides all the algorithms needed to calculate navigation data output.

Figure 3 shows the block diagram for the baseband-IC. Selected functional blocks are described in the following sections.

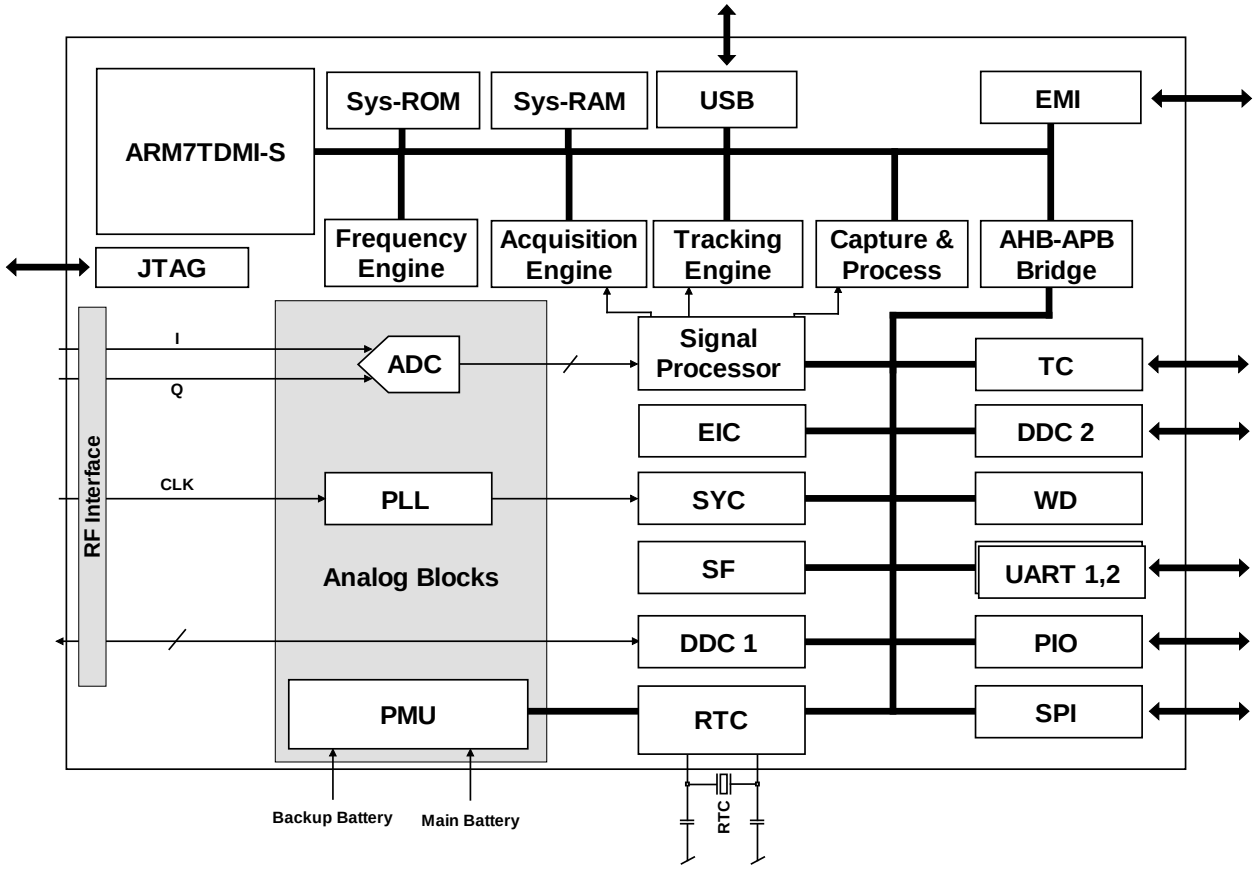


Figure 3: u-blox 6 Baseband-IC block diagram

2.1 Process engines

2.1.1 Capture & Process

The Capture & Process functional block supports u-blox' Capture & Process technology (see section 1.9).

2.2 Peripherals

A number of peripheral interfaces are provided. The embedded firmware uses these interfaces according to their respective protocol specifications. For specific applications, the firmware also supports the connection of peripheral devices, such as external memories or sensors, to some of the interfaces.

2.2.1 UART

The baseband-IC has two UART interfaces, both of which can be used for position transmission. These ports support NMEA and UBX protocols at different baud rates. The useable low end baudrates depend on user requested communication traffic. For supported baudrates see the *u-blox 5 & u-blox 6 Receiver Description Including Protocol Specification* [2].

The UART configuration can be defined at system start-up through configuration pins or settings stored permanently in any non-volatile memory attached to the baseband-IC. Note that only one UART is available on the UBX-G6010.

2.2.2 USB

A USB version 2.0 FS (Full Speed, 12Mbit/s) interface can be used as an alternative to the UART. The pull-up resistor on DP is integrated to signal a full-speed device to the host. The VDD_USB pin supplies the USB interface, independently from the VDD_IO pin.

2.2.3 SPI

The SPI allows for the connection of external devices with a serial interface, e.g. FLASH memories or A/D converters, or to interface to a host CPU. The interface can be operated in master or slave mode. In master mode, one chip select signal is available to select external slaves. In slave mode a single chip select signal enables communication with the host.

SPI FLASH is supported for AssistNow Offline data and to store the receiver configuration.

2.2.4 Display Data Channel (DDC)

Two independent DDC interfaces are available. One is used exclusively for communication with the RF-IC.

The second interface can be used either to access external devices with a serial interface, e.g. EEPROM or A/D converters, or to interface with a host CPU. It is capable of master and slave operation. The DDC protocol and electrical interface are fully compatible with Standard-Mode of the I^2C industry standard.

2.2.5 Peripheral Input Output (PIO)

The PIO block has two basic functions:

- It maps peripheral functions to the I/O pins. The configuration of the pin is determined by the peripheral function.
- It allows the use of I/O pins as general-purpose I/O.

Optionally pull-up or pull-down resistors can be enabled separately for each pin.

2.2.6 External Memory Interface (EMI)

The external memory interface is used to connect to external FLASH memory. Up to 32 Mbit size 16-bit wide memories can be connected. Address lines EM_A18…EM_A21 are shared with PIO functions. EMI is only available with the UBX-G6000-B.

2.2.7 Real-Time Clock (RTC) with backup RAM

The RTC is driven by its own 32 kHz oscillator and is, together with the 4 KB backup RAM, powered by the VDD_B back-up supply voltage. When the engine is in a power-saving mode or when the battery is low, part of the baseband switches off. The RTC provides a timing reference at these times, which enables all relevant data to be saved in the backup RAM to allow later a Hot-Start.

The RTC crystal is optional as it is required in stand-alone applications where hot or warm starts are enabled. It is also required for using Power Save Mode. In these cases, actual time is maintained in the RTC and Ephemeris and other last known data is kept in the backup RAM. In A-GPS based systems, the RTC is not required and coarse or fine time information is available from the network. If neither backup RAM nor RTC are required, V_BCKP should be connected to GND.

2.2.8 Watchdog (WD)

u-blox 6 includes a Watchdog timer, that prevents system-lockups caused when the software gets trapped in a deadlock. During normal operation, the firmware resets the watchdog's internal counter at regular intervals before timer overflow occurs.

2.2.9 Special Function Register (SF)

This register contains chip version and boot configuration read from SAFEBOOT_N and CFG_PIN pins.

2.2.10 Timer Counter (TC)

Timer counter has two TIMEMARK inputs and two TIMEPULSE outputs.

TIMEMARK inputs (routed through EXTINT0 and EXTINT1) time external events relative to GPS time.

TIMEPULSE outputs generate pulse trains synchronized with GPS or UTC time grid with intervals configurable over a wide frequency range. Thus one TIMEPULSE output may be used as a low frequency time synchronization pulse while the other is being used as a high frequency reference frequency.

All in- and output signals are synchronized with the receiver internal clock frequency of 48 MHz, resulting in an inherent maximum quantization error of in- and output signals of +/- 10 ns.

2.3 Analog blocks

2.3.1 Phase Lock Loop (PLL)

The fully integrated low-power fractional sigma-delta PLL generates the master clock frequency from a wide selection range of reference frequencies supplied at the differential CLK input.

2.3.2 Power Management Unit (PMU)

The PMU provides all required supply voltages to the system. A number of configurations are possible:

- A single supply voltage can be used for the complete system.
- The RF and baseband sections can be supplied by different voltage sources.

The PMU also generates the supply voltage for the TCXO, if used. However the TCXO specification may affect the system supply voltage range.

When the battery level is too low for proper system operation, the PMU will automatically switch off all blocks but the backup section of the baseband-IC containing the RTC and the backup RAM. A separate backup-battery may be connected to the baseband for supplying V_BCKP in case the main voltage V_RUN is not available.

3 RF subsystem

The RF-IC receiver implements a low-IF architecture with a 3 MHz intermediate frequency. The input signal is a 6MHz wide portion of the spectrum centered on the L1 GPS/GALILEO band at 1575.42 MHz. The received signal is amplified by a single-ended 50 Ohm-matched low-noise amplifier, and then fed to an external SAW filter with a 50 Ohm input impedance. The SAW filter provides a single-ended to differential conversion and has a 100 Ohm differential output impedance. A differential RF amplifier, input matched to 100 Ohm, offers further amplification, thus reducing the noise figure requirements for the I and Q mixers. After down-conversion, the I and Q signals are low-pass filtered and amplified by a Programmable Gain Amplifier (PGA). The differential I and Q signals are then sent to the baseband IC, where A/D conversion, signal processing and final image rejection are performed.

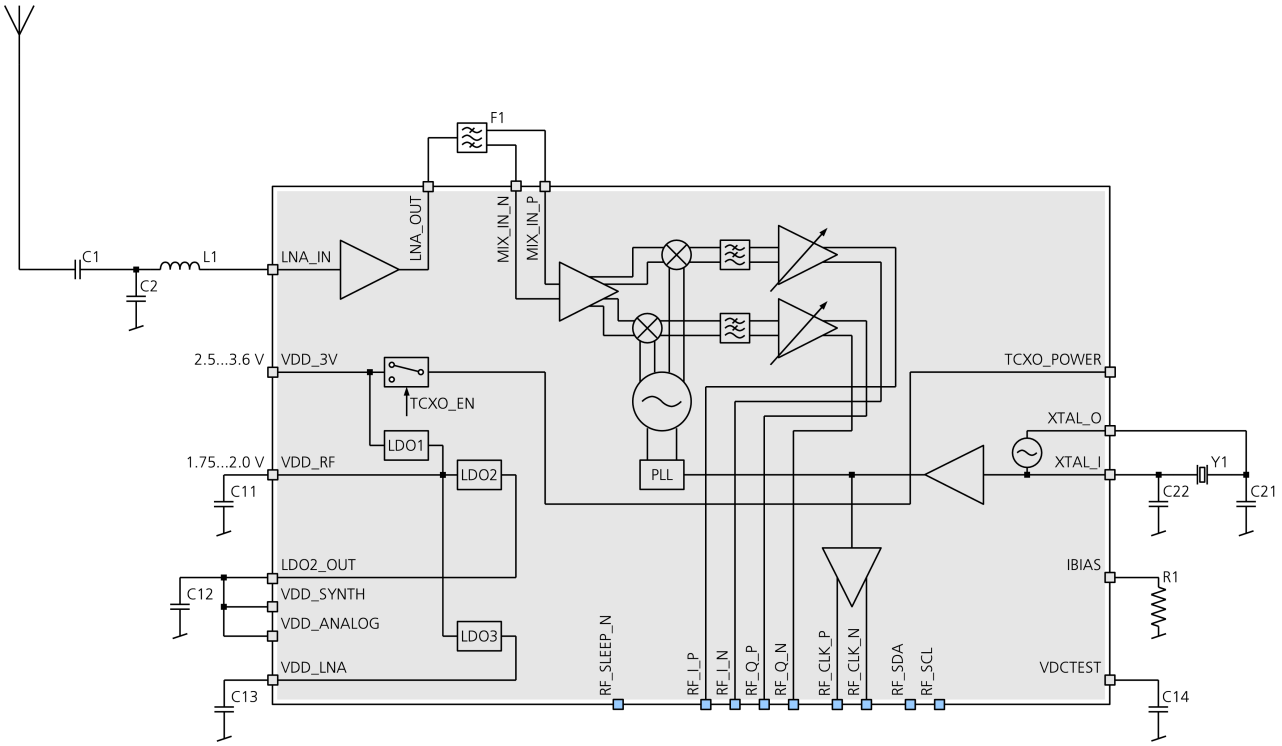


Figure 4: RF IC block diagram

4 Power management and operating modes

4.1 Operating modes

u-blox-6 ICs have 2 continuous operating modes (Maximum Performance Mode and Eco Mode) and 1 intermittent operating mode (Power Save Mode). Maximum Performance Mode freely uses the acquisition engine, resulting in the best possible TTFF, while Eco Mode optimizes the use of the acquisition engine to deliver lower current consumption. At medium to strong signals, there is almost no difference for acquisition and tracking performance in these modes.

4.1.1 Maximum Performance Mode

In Maximum Performance mode, u-blox 6 receivers use the acquisition engine at full performance to search for all possible satellites until the Almanac is completely downloaded.

As a consequence, tracking current consumption level will be achieved when:

- A valid GPS position is fixed
- Almanac is entirely downloaded
- Ephemeris for all satellites in view are valid

4.1.2 Eco Mode

In Eco Mode, u-blox 6 receivers use the acquisition engine to search for new satellites only when needed for navigation:

- In cold starts, u-blox 6 searches for enough satellites to navigate and optimizes use of the acquisition engine to download their ephemeris.
- In non-cold starts, u-blox 6 focuses on searching for visible satellites whose orbits are known from the Almanac.

In Eco Mode, the u-blox 6 acquisition engine limits use of its searching resources to minimize power consumption. As a consequence the time to find some satellites at weakest signal level might be slightly increased in comparison to Maximum Performance Mode.

u-blox 6 deactivates the acquisition engine as soon as a position is fixed and a sufficient number (at least 4) of satellites are being tracked. The tracking engine continues to search and track new satellites without orbit information.

4.1.3 Power Save Mode

u-blox 6 ICs include power saving options that allow reducing the average tracking current consumption by periodically switching off parts of or the complete GPS receiver and waking it up at configurable intervals from one second to one week. This can be done by using a hardware interrupt or by sending a serial command.

☞ For more information about power management strategies, see the *u-blox 5 & u-blox 6 Receiver Description Including Protocol Specification* [2] and the *Power Management Considerations Application Note* [4].

4.2 Acquisition configuration

u-blox 6 positioning technology allows configuration of the acquisition engine to a slower update rate, which can reduce power consumption. This can in some situations result in a longer TTFF.

☞ For more information see the u-blox *5 & u-blox 6 Receiver Description Including Protocol Specification* [2].

4.3 Base-band I/O supply voltage (VDD_IO)

The digital I/Os of the baseband part are supplied with VDD_IO from the host system. The wide range of VDD_IO allows seamless interfacing to standard logic voltage levels independently of the baseband supply voltage level. Without VDD_IO supply the system will be kept in reset state.

4.4 Calculating power consumption

See the *Power Management Considerations Application Note* [4].

4.5 External DC/DC converter control

Pin DCDC_EN enables external DC/DC converter.

5 Configuration management

System configuration goes through multiple steps. The hierarchy of the information found at different sources is as follows:

1. Actual configuration in system RAM
2. Configuration in backup RAM
3. Configuration in FLASH memory
4. Configuration in serial EEPROM
5. Configuration through CFG pins
6. Default (ROM) settings

During system boot, the system first starts from the ROM default settings. Then it tries to find out where the actual configuration can be found, i.e. it searches for EEPROM, FLASH and/or backup RAM and looks for valid contents. Thus, a search tree can be built and any configuration setting that is needed by the firmware is searched downwards from the most actual (system RAM) to the most outdated (system ROM) information. The system uses the first valid information it finds.

5.1 Configuration pins

Some PIO pins are read at system start and can be used to submit some start-up configuration into the boot process. In the following tables, all default settings (pin left open) are **bold**.

The first step is to analyze the SAFEBOOT_N pin. If it is pulled to low level, the system will start up in safe mode using as few configuration settings as possible and establishing only the minimum functionality required for establishing communication with the host. No GPS operation is started. This mode is primarily used for production testing.

The state of SAFEBOOT_N at system start is preserved in bit BOOTMODE0 of the special function register (SF).

SAFEBOOT_N	
1	**Normal Boot**
0	Safe Mode, minimal ROM boot, Ignore Backup RAM & FLASH.

Table 4: SAFEBOOT configuration

The CFG_PIN decides whether external parallel FLASH memory is accessed at all. If the CFG_PIN is left open (i.e. = 1) at power up the receiver reads the configuration from the configuration pins.

The detection of serial FLASH on SPI and serial EEPROM on DDC interfaces is not affected by CFG_PIN. In default, only pin configurations will be read.

The state of CFG_PIN at system start is preserved in bit BOOTMODE1 of the special function register (SF).

CFG_PIN	
1	**Use CFG pins**
0	Ignore CFG pins, required setting for parallel Flash

Table 5: Pin configuration

☞ For more information about configuration consult the *UBX-G6010, UBX-G6000/UBX-G0010 Hardware Integration Manual* [1].

CFG_CLK determines GPS clock frequency.

CFG_CLK2	CFG_CLK1	CFG_CLK0	Reference Frequency
1	**1**	**1**	**26 MHz**
1	1	0	38.4 MHz
1	0	1	33.6 MHz
1	0	0	19.2 MHz
0	1	1	16.8 MHz
0	1	0	Reserved
0	0	1	Reserved
0	0	0	Reserved

Table 6: Reference GPS clock configuration

☞ Refer to Table 30 for AC parameter frequency range limitations applicable to XTAL and TCXO operation, respectively.

The communication interfaces (UART1/2, USB, SPI, DDC) can be configured in terms of protocol and baud rate.

CFG_COM1	CFG_COM0	Protocol	Messages	UART1/2 Baud rate	USB Power
1	**1**	**NMEA**	**GSV, RMC, GSA, GGA, GLL, VTG, TXT**	**9600**	**BUS Powered**
1	0	NMEA	GSV, RMC, GSA, GGA, GLL, VTG, TXT	38400	Self Powered
0	1	NMEA	GSV[9], RMC, GSA, GGA, VTG, TXT	4800	BUS Powered
0	0	UBX	NAV-SOL, NAV-STATUS, NAV-SVINFO, NAV-CLOCK, INF, MON-EXCEPT, AID-ALPSERV	57600	BUS Powered

Table 7: COM configuration

The strategy of the GNSS receiver management can be optimized according to several different operation modes. The goal is to adapt power consumption and responsiveness, as well as sensitivity, to a given application.

CFG_GPS2	CFG_GPS1	CFG_GPS0	GPS mode
1	**1**	**1**	**Maximum Performance Mode TCXO**
1	1	0	Eco Mode TCXO
1	0	1	Reserved
1	0	0	Capture & Process boot mode TCXO
0	1	1	Maximum Performance Mode XTO
0	1	0	Eco Mode XTO
0	0	1	Reserved
0	0	0	Capture & Process boot mode XTO

Table 8: GPS operation configuration

There are additional configuration pins reserved for further use, identified by pin name CFG_FFUx. Do not connect these pins unless pins are used for another secondary function.

[9] every 5th fix

6 Pin definition

6.1 Pin assignment

Figure 5/Table 9, Figure 6 and Figure 7 show the pin assignments of the CVBGA, MLF24 and MLF56 chips respectively. Note that the signal names are linked to the corresponding description tables.

Some pins have shared functions. Use special care when designing with these pins since overall function and configuration of the device can be affected.

6.1.1 CVBGA100 / UBX-G6000-B

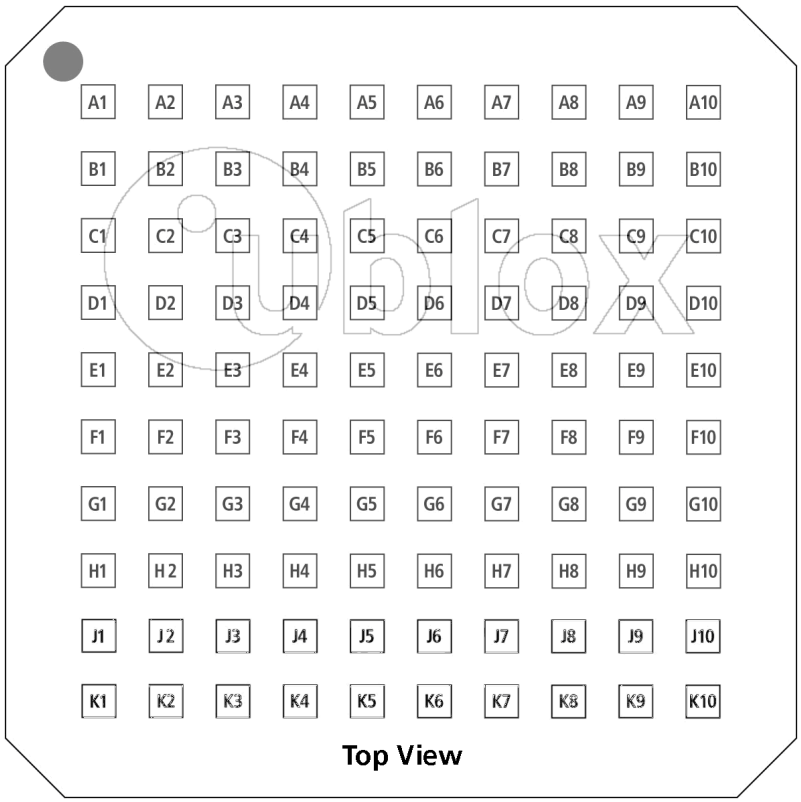


Figure 5: CVBGA (UBX-G6000-B) top view

	1	2	3	4	5	6	7	8	9	10
A	RTC_XTAL_I	BB_SLEEP_N	BB_CLK_P	BB_I_N	BB_Q_N	EM_A9	EM_D8	CFG_PIN / TMS	EM_A6	TCK
B	RTC_XTAL_O	VSS_PLL	BB_CLK_N	BB_I_P	BB_Q_P	EM_D15	EM_D9	EM_A7	PIO13 / CFG_CLK0 / EM_A0	PIO17 / CFG_FFU2 / EM_A20
C	VDD_PLL	EM_D11	PIO23 / CFG_GPS2	PIO0 / BB_SDA	Not connected	WE_N	EM_A3	TIMEPULSE / TDO	SAFEBOOT_N / TDI	EM_A2
D	EM_A11	PIO22 / CFG_GPS1	PIO1 BB_SCL	Not connected	PIO7 / EXTINT0	PIO8 / EXTINT1	EM_A5	CS2_N	EM_A1	OE_N
E	EM_A10	EM_A12	GND	GND	GND	GND	EM_D10	VDD_IO1	EM_A4	PIO16 / CFG_FFU0 / EM_A19
F	EM_A14	EM_A15	EM_D14	EM_D4	GND	GND	GND	PIO6 / SS_N / SCS0_N	PIO14 / CFG_CLK1	PIO15 / CFG_CLK2 / EM_A18
G	EM_A16	PIO12 / ANT_SHORT_N / RXD2	VDD_USB	EM_A8	EM_D6	PIO9 / PER_RESET_N	PIO4 / RXD1	VDD_C1	EM_D0	PIO24 / CFG_FFU1
H	PIO10 / ANT_DETECT	PIO11/ ANT_OFF / TXD2	EM_A17	PIO18 / CFG_FFU3 / EM_A21 / TIMEPULSE2	EM_D5	PIO5 / TXD1	Do not connect	PIO2 / SDA2	EM_D7	PIO3 / SCL2
J	EM_A13	USB_DM	VDD_C0	EM_D12	EM_D3	EM_D1	V_RESET	DCDC_EN	V_RUN	PIO19 / CFG_COM0 / MOSI
K	USB_DP	VDD_IO0	EM_D13	PIO20 / CFG_COM1 / MISO	PIO21 / CFG_GPS0 / SCK	EM_D2	V_TH	V_DCDC	V_BCKP	VDD_B

Table 9: Pin assignment CVBGA (UBX-G6000)

6.1.2 MLF24 / UBX-G0010-Q

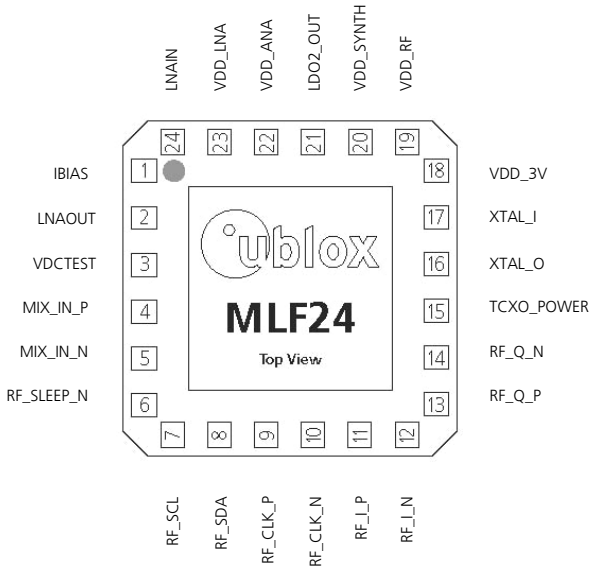


Figure 6: Pin assignment MLF24 (UBX-G0010-Q)

☞ Signal names are linked to the corresponding description tables. For multiple function pins, select the specific signal.

6.1.3 MLF56 / UBX-G6010-S

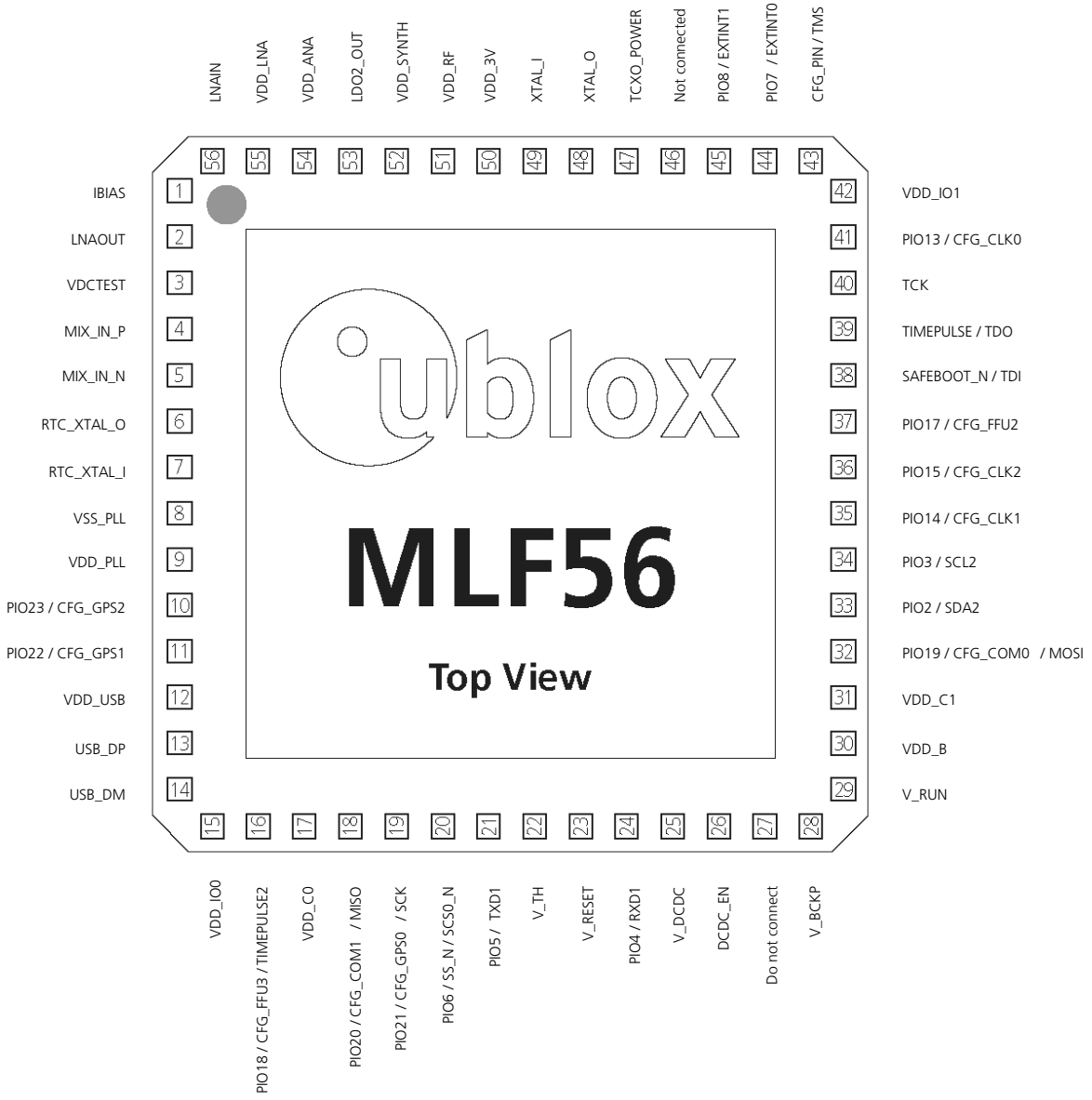


Figure 7: Pin assignment MLF56 (UBX-G6010-S)

☞ Signal names are linked to the corresponding description tables. For multiple function pins, select the specific signal.

6.2 Pin description

Name	Pin CVBGA	Pin MLF56	Pin MLF24	Power Domain	I/O Reset	I/O Core off	Description
V_DCDC	K8	25	-	VDD_B			Main Core Supply
V_RUN	J9	29	-	VDD_B			Main Backup Supply
V_BCKP	K9	28	-	VDD_B			Backup Cell Supply
VDD_B	K10	30	-	VDD_B			Backup Power
VDD_C0	J3	17	-	VDD_C			Core Power
VDD_C1	G8	31	-	VDD_C			Core Power
VDD_IO0	K2	15	-	VDD_IO			I/O Ring Power
VDD_IO1	E8	42	-	VDD_IO			I/O Ring Power
VDD_USB	G3	12	-	VDD_USB			USB Power
VDD_PLL	C1	9	-	VDD_PLL			PLL Power
V_RESET	J7	23	-	VDD_B			Supply Monitor Analog
V_TH	K7	22	-	VDD_B			Reset Threshold Analog
DCDC_EN	J8	26	-	VDD_IO	Output Low	Input Pull-Down	DC/DC Control Output
VSS_B0	E3, E4, E5, E6, F5, F6, F7	Center GND Pad	-	VDD_B			Ground
VSS_B1			-	VDD_B			Ground
VSS_C0			-	VDD_C			Ground
VSS_C1			-	VDD_C			Ground
VSS_C2			-	VDD_C			Ground
VSS_IO0			-	VDD_IO			Ground
VSS_IO1			-	VDD_IO			Ground
VSS_USB			-	VDD_USB			Ground
VSS_RF	-		Center GND Pad				Ground
VSS_PLL	B2	8	-				PLL Analog Reference Ground
IBIAS	-	1	1				Reference Current Analog
LDO2_OUT	-	53	21				LDO2 Output
TCXO_POWER	-	47	15				TCXO Bias Current
VDD_3V	-	50	18				RF Main Supply
VDD_ANA	-	54	22				Analog Power
VDD_LNA	-	55	23				LNA Power Supply
VDD_RF	-	51	19				RF Core Power
VDD_SYNTH	-	52	20				Synthesizer Power

Table 10: Power Management

Name	Pin CVBGA	Pin MLF56	Pin MLF24	Power Domain	I/O Reset	I/O Pwr off	Description
BB_I_P	B4	-	-	VDD_IO / VDD_C	Input	Input	Analog I Channel Differential Input
BB_I_N	A4	-	-	VDD_IO / VDD_C	Input	Input	Analog I Channel Differential Input
BB_Q_P	B5	-	-	VDD_IO / VDD_C	Input	Input	Analog Q Channel Differential Input
BB_Q_N	A5	-	-	VDD_IO / VDD_C	Input	Input	Analog Q Channel Differential Input
BB_CLK_P	A3	-	-	VDD_IO / VDD_C	Input	Input	Analog CLK Channel Differential Input
BB_CLK_N	B3	-	-	VDD_IO / VDD_C	Input	Input	Analog CLK Channel Differential Input
BB_SLEEP_N	A2	-	-	VDD_IO	Output Low	Input Pull-down	Output RF Sleep
PIO0 / BB_SDA	C4	-	-	VDD_IO	Input Pull-up	Input Pull-up	I/O DDC for RF control Serial Data Shared with PIO0
PIO1 / BB_SCL	D3	-	-	VDD_IO	Input Pull-up	Input Pull-up	I/O DDC for RF control Serial Clock Shared with PIO1
RF_CLK_N	-	-	10	VDD_ANA	Output	Output	Analog CLK Differential Output
RF_CLK_P	-	-	9	VDD_ANA	Output	Output	Analog CLK Differential Output
RF_I_N	-	-	12	VDD_ANA	Output	Output	Analog I-Channel Differential Output
RF_I_P	-	-	11	VDD_ANA	Output	Output	Analog I-Channel Differential Output
RF_Q_N	-	-	14	VDD_ANA	Output	Output	Analog Q-Channel Differential Output
RF_Q_P	-	-	13	VDD_ANA	Output	Output	Analog Q-Channel Differential Output
RF_SCL	-	-	7	VDD_RF	Input	Input	I/O DDC for RF control Serial Clock
RF_SDA	-	-	8	VDD_RF	Input	Input	I/O DDC for RF control Serial Data
RF_SLEEP_N	-	-	6	VDD_RF	Input	Input	Input RF Sleep

Table 11: RF/BB interface

Name	Pin CVBGA	Pin MLF56	Pin MLF24	Power Domain	I/O Reset	I/O Pwr off	Description
LNAIN	-	56	24	VDD_LNA	Input	Input	LNA Input
LNAOUT	-	2	2	VDD_LNA	Output	Output	LNA Output
MIX_IN_N	-	5	5	VDD_ANA	Input	Input	Mixer Differential Input
MIX_IN_P	-	4	4	VDD_ANA	Input	Input	Mixer Differential Input
XTAL_I	-	49	17	VDD_SYN	Input	Input	XTO Input
XTAL_O	-	48	16	VDD_SYN	Output	Output	XTO Output

Table 12: RF Analog

Name	Pin CVBGA	Pin MLF56	Pin MLF24	Power Domain	I/O Reset	I/O Pwr off	Description
RTC_XTAL_O	B1	6	-	VDD_B	Output	Output	Output RTC
RTC_XTAL_I	A1	7	-	VDD_B	Input	Input	Input RTC
TCK	A10	40	-	VDD_IO	Input Pull-up	Input Pull-up	Input JTAG Test Clock
SAFEBOOT_N / TDI	C9	38	-	VDD_IO	Input Pull-up	Input Pull-up	Input JTAG Test Data In Shared with Safe Boot Mode (Table 4)
TIMEPULSE / TDO	C8	39	-	VDD_IO	Output low	Input Pull-up	Output JTAG Data Out Shared with Time Pulse
CFG_PIN / TMS	A8	43	-	VDD_IO	Input Pull-up	Input Pull-up	Input JTAG Test Mode Select Shared with CFG_PIN (Table 5)
VDCTEST	-	3	3				Analog RF test pin
PIO9 / PER_RESET_N	G6	-	-	VDD_IO	Output low	Input Pull-down	Output Peripheral Reset Shared with PIO9

Table 13: System

Name	Pin CVBGA	Pin MLF56	Pin MLF24	Power Domain	I/O Reset	I/O Pwr off	Description
USB_DM	J2	14	-	VDD_USB	Input	Input	I/O Differential USB D-
USB_DP	K1	13	-	VDD_USB	Input	Input	I/O Differential USB D+

Table 14: USB

Name	Pin CVBGA	Pin MLF56	Pin MLF24	Power Domain	I/O Reset	I/O Pwr off	Description
PIO2 / SDA2	H8	33	-	VDD_IO	Input Pull-up	Input Pull-up	I/O DDC for peripherals Serial Data Shared with PIO2
PIO3/ SCL2	H10	34	-	VDD_IO	Input Pull-up	Input Pull-up	I/O DDC for peripherals Serial Clock Shared with PIO3

Table 15: DDC

Name	Pin CVBGA	Pin MLF56	Pin MLF24	Power Domain	I/O Reset	I/O Pwr off	Description
PIO4 / RXD1	G7	24	-	VDD_IO	Input Pull-Up	Input Pull-Up	Input UART 1 RxD Shared with PIO4
PIO5 / TXD1	H6	21	-	VDD_IO	Input Pull-up	Input Pull-up	Output UART 1 TxD Shared with PIO5
PIO11/ ANT_OFF / TXD2	H2	-	-	VDD_IO	Input Pull-up	Input Pull-up	Output UART 2 TxD Shared with ANT_OFF Shared with PIO11
PIO12/ ANT_SHORT_ N / RXD2	G2	-	-	VDD_IO	Input Pull-up	Input Pull-up	Input UART 2 RxD Shared with ANT_SHORT Shared with PIO12

Table 16: Asynchronous serial interface (UART)

Name	Pin CVBGA	Pin MLF56	Pin MLF24	Power Domain	I/O Reset	I/O Pwr off	Description
PIO6 SS_N / SCS0_N	F8	20	-	VDD_IO	Input Pull-up	Input Pull-up	I/O SPI Chip/Slave Select Shared with PIO6
PIO19 CFG_COM0 / MOSI	J10	32	-	VDD_IO	Input Pull-up	Input Pull-up	I/O SPI MOSI Shared with CFG_COM0 (Table 7) Shared with PIO19
PIO20 / CFG_COM1 / MISO	K4	18	-	VDD_IO	Input Pull-up	Input Pull-up	I/O SPI MISO Shared with CFG_COM1 (Table 7) Shared with PIO20
PIO21 / CFG_GPS0 / SCK	K5	19	-	VDD_IO	Input Pull-up	Input Pull-up	I/O SPI Clock Shared with CFG_GPS0 (Table 8) Shared with PIO21

Table 17: SPI

Name	Pin CVBGA	Pin MLF56	Pin MLF24	Power Domain	I/O Reset	I/O Pwr off	Description
PIO7 / EXTINT0	D5	44	-	VDD_IO	Input Pull-up	Input Pull-up	Input External Interrupt / Time Mark 0 Shared with PIO7
PIO8 / EXTINT1	D6	45	-	VDD_IO	Input Pull-up	Input Pull-up	Input External Interrupt / Time Mark 1 Shared with PIO8
TIMEPULSE / TDO	C8	39	-	VDD_IO	Output low	Input Pull-up	Output Time Pulse Shared with JTAG Test Data Out
PIO18 / CFG_FFU3 / EM_A21 / TIMEPULSE2	H4	16	-	VDD_IO	Input Pull-up	Input Pull-up	Output Time Pulse 2 Shared with EM_A21 on CVBGA Shared with CFG_FFU3 (for further use) Shared with PIO18

Table 18: External Interrupt / Time Mark

Name	Pin CVBGA	Pin MLF56	Pin MLF24	Power Domain	I/O Reset	I/O Pwr off	Description
PIO10/ ANT_DETECT	H1	-	-	VDD_IO	Input Pull-up	Input Pull-up	Input Active Antenna Detection Shared with PIO10
PIO11/ ANT_OFF / TXD2	H2	-	-	VDD_IO	Input Pull-up	Input Pull-up	Output Active Antenna Off Shared with UART 2 TxD Shared with PIO11
PIO12/ ANT_SHORT_ N / RXD2	G2	-	-	VDD_IO	Input Pull-up	Input Pull-up	Input Active Antenna Short Detection Shared with UART 2 RxD Shared with PIO12

Table 19: Antenna supervisor

Name	Pin CVBGA	Pin MLF56	Pin MLF24	Power Domain	I/O Reset	I/O Pwr off	Description
PIO13 / CFG_CLK0 / EM_A0	B9	41	-	VDD_IO	Input Pull-up	Input Pull-up	Input CFG_CLK0 (Table 6) Shared with EM_A0 on CVBGA Shared with PIO13
PIO14 / CFG_CLK1	F9	35	-	VDD_IO	Input Pull-up	Input Pull-up	Input CFG_CLK1 (Table 6) Shared with PIO14
PIO15 / CFG_CLK2 / EM_A18	F10	36	-	VDD_IO	Input Pull-up	Input Pull-up	Input CFG_CLK2 (Table 6) Shared with EM_A18 on CVBGA Shared with PIO15
PIO16 / CFG_FFU0 / EM_A19	E10	-	-	VDD_IO	Input Pull-up	Input Pull-up	Input CGF_FFU0 (for further use) Shared with EM_A19 Shared with PIO 16
PIO17 / CFG_FFU2 / EM_A20	B10	37	-	VDD_IO	Input Pull-up	Input Pull-up	Input CGF_FFU2 (for further use) Shared with EM_A20 on CVBGA Shared with PIO17
PIO18 / CFG_FFU3 / EM_A21 / TIMEPULSE2	H4	16	-	VDD_IO	Input Pull-up	Input Pull-up	Input CGF_FFU3 (for further use) Shared with EM_A21 on CVBGA Shared with Time Pulse 2 Shared with PIO18
PIO19 / CFG_COM0 / MOSI	J10	32	-	VDD_IO	Input Pull-up	Input Pull-up	Input CFG_COM0 (Table 7) Shared with SPI MOSI Shared with PIO19
PIO20 / CFG_COM1 / MISO	K4	18	-	VDD_IO	Input Pull-up	Input Pull-up	Input CFG_COM1 (Table 7) Shared with SPI MISO Shared with PIO20
PIO21 / CFG_GPS0 / SCK	K5	19	-	VDD_IO	Input Pull-up	Input Pull-up	Input CFG_GPS0 (Table 8) Shared with SPI SCK Shared with PIO21
PIO22 / CFG_GPS1	D2	11	-	VDD_IO	Input Pull-up	Input Pull-up	Input CFG_GPS1 (Table 8) Shared with PIO22
PIO23 / CFG_GPS2	C3	10	-	VDD_IO	Input Pull-up	Input Pull-up	Input CFG_GPS2 (Table 8) Shared with PIO23.
PIO24 / CFG_FFU1	G10	-	-	VDD_IO	Input Pull-up	Input Pull-up	Input CFG_FFU0 (for further use) Shared with PIO24
CFG_PIN / TMS	A8	43	-	VDD_IO	Input Pull-up	Input Pull-up	Input CFG_PIN (Table 5) Shared with JTAG Test Mode Select
SAFEBOOT_N / TDI	C9	38	-	VDD_IO	Input Pull-up	Input Pull-up	Input Safe Boot Mode (Table 4) Shared with JTAG Test Data In

Table 20: Configuration

Name	Pin CVBGA	Pin MLF56	Pin MLF24	Power Domain	I/O Reset	I/O Pwr off	Description
EM_D0	G9	-	-	VDD_IO	Input Pull-up	Input Pull-up	I/O Data Bus D0
EM_D1	J6	-	-	VDD_IO	Input Pull-up	Input Pull-up	I/O Data Bus D1
EM_D2	K6	-	-	VDD_IO	Input Pull-up	Input Pull-up	I/O Data Bus D2
EM_D3	J5	-	-	VDD_IO	Input Pull-up	Input Pull-up	I/O Data Bus D3
EM_D4	F4	-	-	VDD_IO	Input Pull-up	Input Pull-up	I/O Data Bus D4
EM_D5	H5	-	-	VDD_IO	Input Pull-up	Input Pull-up	I/O Data Bus D5
EM_D6	G5	-	-	VDD_IO	Input Pull-up	Input Pull-up	I/O Data Bus D6
EM_D7	H9	-	-	VDD_IO	Input Pull-up	Input Pull-up	I/O Data Bus D7
EM_D8	A7	-	-	VDD_IO	Input Pull-up	Input Pull-up	I/O Data Bus D8
EM_D9	B7	-	-	VDD_IO	Input Pull-up	Input Pull-up	I/O Data Bus D9
EM_D10	E7	-	-	VDD_IO	Input Pull-up	Input Pull-up	I/O Data Bus D10
EM_D11	C2	-	-	VDD_IO	Input Pull-up	Input Pull-up	I/O Data Bus D11
EM_D12	J4	-	-	VDD_IO	Input Pull-up	Input Pull-up	I/O Data Bus D12
EM_D13	K3	-	-	VDD_IO	Input Pull-up	Input Pull-up	I/O Data Bus D13
EM_D14	F3	-	-	VDD_IO	Input Pull-up	Input Pull-up	I/O Data Bus D14
EM_D15	B6	-	-	VDD_IO	Input Pull-up	Input Pull-up	I/O Data Bus D15
PIO13 / CFG_CLK0 / EM_A0	B9	-	-	VDD_IO	Input Pull-up	Input Pull-up	Output Address Bus A0 Shared with CFG_CLK0 (Table 6) Shared with PIO13
EM_A1	D9	-	-	VDD_IO	Output low	Input Pull-down	Output Address Bus A1
EM_A2	C10	-	-	VDD_IO	Output low	Input Pull-down	Output Address Bus A2
EM_A3	C7	-	-	VDD_IO	Output low	Input Pull-down	Output Address Bus A3
EM_A4	E9	-	-	VDD_IO	Output low	Input Pull-down	Output Address Bus A4
EM_A5	D7	-	-	VDD_IO	Output low	Input Pull-down	Output Address Bus A5
EM_A6	A9	-	-	VDD_IO	Output low	Input Pull-down	Output Address Bus A6
EM_A7	B8	-	-	VDD_IO	Output low	Input Pull-down	Output Address Bus A7
EM_A8	G4	-	-	VDD_IO	Output low	Input Pull-down	Output Address Bus A8
EM_A9	A6	-	-	VDD_IO	Output low	Input Pull-down	Output Address Bus A9
EM_A10	E1	-	-	VDD_IO	Output low	Input Pull-down	Output Address Bus A10
EM_A11	D1	-	-	VDD_IO	Output low	Input Pull-down	Output Address Bus A11

Name	Pin CVBGA	Pin MLF56	Pin MLF24	Power Domain	I/O Reset	I/O Pwr off	Description
EM_A12	E2	-	-	VDD_IO	Output low	Input Pull-down	Output Address Bus A12
EM_A13	J1	-	-	VDD_IO	Output low	Input Pull-down	Output Address Bus A13
EM_A14	F1	-	-	VDD_IO	Output low	Input Pull-down	Output Address Bus A14
EM_A15	F2	-	-	VDD_IO	Output low	Input Pull-down	Output Address Bus A15
EM_A16	G1	-	-	VDD_IO	Output low	Input Pull-down	Output Address Bus A16
EM_A17	H3	-	-	VDD_IO	Output low	Input Pull-down	Output Address Bus A17
PIO15 / CFG_CLK2 / EM_A18	F10	-	-	VDD_IO	Input Pull-up	Input Pull-up	Output Address Bus A18 Shared with CFG_CLK2 (Table 6) Shared with PIO15
PIO16 / CFG_FFU0 / EM_A19	E10	-	-	VDD_IO	Input Pull-up	Input Pull-up	Output Address Bus A19 Shared with CFG_FFU0 (for further use) Shared with PIO16
PIO17 / CFG_FFU2 / EM_A20	B10	-	-	VDD_IO	Input Pull-up	Input Pull-up	Output Address Bus A20 Shared with CFG_FFU2 (for further use) Shared with PIO17
PIO18 / CFG_FFU3 / EM_A21 / TIMEPULSE2	H4	-	-	VDD_IO	Input Pull-up	Input Pull-up	Output Address Bus A21 Shared with Time Pulse 2 Shared with CFG_FFU3 (for further use) Shared with PIO18
CS2_N	D8	-	-	VDD_IO	Output high	Input Pull-up	Output Chip Select 2
OE_N	D10	-	-	VDD_IO	Output high	Input Pull-up	Output Output Enable
WE_N	C6	-	-	VDD_IO	Output high	Input Pull-up	Output Write Enable

Table 21: EMI (only on CVBGA)

Name	Pin CVBGA	Pin MLF56	Pin MLF24	Power Domain	I/O Reset	I/O Pwr off	Description
PIO0 / BB_SDA	C4	-	-	VDD_IO	Input Pull-up	Input Pull-up	I/O PIO0 Shared with DDC for RF Serial Data
PIO1 / BB_SCL	D3	-	-	VDD_IO	Input Pull-up	Input Pull-up	I/O PIO1 Shared with DDC for RF Serial Clock
PIO2 / SDA2	H8	33	-	VDD_IO	Input Pull-up	Input Pull-up	I/O PIO2 Shared with DDC for peripherals Serial Data
PIO3 / SCL2	H10	34	-	VDD_IO	Input Pull-up	Input Pull-up	I/O PIO3 Shared with DDC for peripherals Serial Clock
PIO4 / RXD1	G7	24	-	VDD_IO	Input Pull-ip	Input Pull-up	I/O PIO4 Shared with UART 1 RxD
PIO5 / TXD1	H6	21	-	VDD_IO	Input Pull-up	Input Pull-up	I/O PIO5 Shared with UART 1 TxD
PIO6 / SS_N / SCS0_N	F8	20	-	VDD_IO	Input Pull-up	Input Pull-up	I/O PIO6 Shared with SPI Slave/Chip Select
PIO7 / EXTINT0	D5	44	-	VDD_IO	Input Pull-up	Input Pull-up	I/O PIO7 Shared with External Interrupt / Time Mark 0
PIO8 / EXTINT1	D6	45	-	VDD_IO	Input Pull-up	Input Pull-up	I/O PIO8 Shared with External Interrupt / Time Mark 1
PIO9 / PER_RESET_N	G6	-	-	VDD_IO	Output low	Input pull-down	I/O PIO9 Shared with Peripheral Reset
PIO10 / ANT_DETECT	H1	-	-	VDD_IO	Input Pull-up	Input Pull-up	I/O PIO10 Shared with antenna supervisor
PIO11 ANT_OFF / TXD2	H2	-	-	VDD_IO	Input Pull-up	Input Pull-up	I/O PIO11 Shared with Active Antenna Off Shared with UART 2 TxD
PIO12 / ANT_SHORT_ N / RXD2	G2	-	-	VDD_IO	Input Pull-up	Input Pull-up	I/O PIO12 Shared with Active Antenna Short Detection Shared with UART 2 RxD
PIO13 / CFG_CLK0 / EM_A0	B9	41	-	VDD_IO	Input Pull-up	Input Pull-up	I/O PIO13 Shared with CFG_CLK0 (Table 6) Shared with EM_A0 on CVBGA
PIO14 / CFG_CLK1	F9	35	-	VDD_IO	Input Pull-up	Input Pull-up	I/O PIO14 Shared with CFG_CLK1(Table 6)
PIO15 / CFG_CLK2 / EM_A18	F10	36	-	VDD_IO	Input Pull-up	Input Pull-up	I/O PIO15 Shared with CFG_CLK2 (Table 6) Shared with EM_A18 on CVBGA
PIO16 / CFG_FFU0 / EM_A19	E10	-	-	VDD_IO	Input Pull-up	Input Pull-up	I/O PIO16 Shared with CFG_FFU2 (for further use) Shared with EM_A19
PIO17 / CFG_FFU2 / EM_A20	B10	37	-	VDD_IO	Input Pull-up	Input Pull-up	I/O PIO17 Shared with CFG_FFU2 (for further use) Shared with EM_A20 on CVBGA
PIO18 / CFG_FFU3 / EM_A21 / TIMEPULSE2	H4	16	-	VDD_IO	Input Pull-up	Input Pull-up	I/O PIO18 Shared with CFG_FFU3 (for further use) Shared with EM_A21 on CVBGA Shared with Time Pulse 2
PIO19 / CFG_COM0 / MOSI	J10	32	-	VDD_IO	Input Pull-up	Input Pull-up	I/O PIO19 Shared with CFG_COM0 (Table 7) Shared with SPI MOSI
PIO20 / CFG_COM1 / MISO	K4	18	-	VDD_IO	Input Pull-up	Input Pull-up	I/O PIO20 Shared with CFG_COM1 (Table 7) Shared with SPI MISO

Name	Pin CVBGA	Pin MLF56	Pin MLF24	Power Domain	I/O Reset	I/O Pwr off	Description
PIO21 / CFG_GPS0 / SCK	K5	19	-	VDD_IO	Input Pull-up	Input Pull-up	I/O PIO21 Shared with CFG_GPS0 (Table 8) Shared with SPI SCK
PIO22 / CFG_GPS1	D2	11	-	VDD_IO	Input Pull-up	Input Pull-up	I/O PIO22 Shared with CFG_GPS1 (Table 8)
PIO23 / CFG_GPS2	C3	10	-	VDD_IO	Input Pull-up	Input Pull-up	I/O PIO23 Shared with CFG_GPS2 (Table 8)
PIO24 / CFG_FFU1	G10	-	-	VDD_IO	Input Pull-up	Input Pull-up	I/O PIO24 Shared with CFG_FFU1 (for further use)

Table 22: PIO

7 Electrical specification

☞ Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

☞ Where application information is given, it is advisory only and does not form part of the specification. For more information regarding power management see the *UBX-G6010, UBX-G6000/UBX-G0010 Hardware Integration Manual* [1].

7.1 Absolute maximum rating

Symbol	Parameter	Condition	Min.	Max.	Unit
VDD_Cx, VDD_B, VDD_PLL	Supply Voltage digital cores (outputs)		-0.5	1.6	V
VDD_IOx	Supply Voltage I/O ring		-0.5	3.6	V
VDD_USB	Supply Voltage USB		-0.5	3.6	V
VDD_RF	Supply Voltage RF Front-end		-0.5	3.6	V
Ipin	DC Current through any digital I/O pin (except supplies)			10	mA
I_TCXO	DC Current through pin TCXO_POWER			2.5	mA
Vi	Input Voltage on any pin not belonging to digital I/O with respect to ground		-0.5	VDD[10]+0.5	V
Vi_{DIG}[11]	Input Voltage on digital I/O pin with respect to ground		-0.5	3.6	V
V_DCDC	Supply Voltage Baseband main core LDO input		-0.5	3.6	V
V_RUN V_BCKP V_RESET V_TH	Supply Voltage Baseband backup core LDO inputs Supply Voltage Baseband backup core LDO inputs Input Voltage Reset Monitor Input Voltage Reset Threshold level		-0.5	3.6	V
VDD_3V	Input Voltage RF LDO		-0.5	3.6	V
Prfin	RF Input Power on LNA_IN, MIX_IN_P, MIX_IN_N			-5	dBm
Ptot	Total Power Dissipation			500	mW
Tjun	Junction Temperature		-40	+105	°C
Ts	Storage Temperature		-40	+125	°C

Table 23: Absolute maximum ratings

[10] VDD is the voltage of the power domain connected to the pin.
[11] Includes the following pins: DCDC_EN, SLEEP_N, PIO0..PIO24, TCK, TDI, TDO, TMS, EM_D0..EM_D15, EM_A1..EM_A17, CS2_N, OE_N, WE_N.

Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. The product is not protected against overvoltage or reversed voltages. If necessary, voltage spikes exceeding the power supply voltage specification, given in table above, must be limited to values within the specified boundaries by using appropriate protection diodes.

7.2 Operating conditions

The test conditions specified in Table 24 apply to all characteristics defined in this section.

Symbol	Parameter	Min.	Typ.	Max.	Unit
Tamb	Ambient Temperature	-40	+25	+85	°C
VSS	Ground		0		V
VDD_Cx, VDD_B, VDD_PLL	Supply Voltage digital core (internally generated)		1.2		V
VDD_IOx	Supply Voltage I/O ring		3.3		V
VDD_USB	Supply Voltage USB		3.3		V
VDD_3V	Supply Voltage RF LDO		3.3		V
VDD_RF	Supply Voltage RF (internally generated)		1.8		V
Fref	Reference Frequency		26		MHz
V_BCKP	Backup Battery Voltage		3		V

Table 24: Test conditions

7.2.1 DC electrical characteristic

For block diagrams of the power supply see the *UBX-G6010, UBX-G6000/UBX-G0010 Hardware Integration Manual* [1].

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD_IOx	Supply voltage I/O ring	1.65	3.3	3.6	V
VDD_USB	Supply voltage USB	3.0	3.3	3.6	V
VDD_3V	Input voltage for VDD_RF LDO	2.5	3.3	3.6	V
V_BCKP	Input voltage for VDD_B LDO (Backup mode)	1.4		3.6	V
V_RUN	Input voltage for VDD_B LDO (Normal mode)	1.4		3.6	V
V_DCDC	Input voltage for VDD_C LDO	1.4		3.6	V
VDD_PLL	Input	1.1	1.2	1.3	V
VDD_RF	VDD_RF LDO output voltage	1.75	1.8	2.0	V

Table 25: Power supply pins

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VDD_3V	Input voltage for VDD_RF LDO		2.5		3.6	V
VDD_B	VDD_B LDO output voltage	LDO1_val_register=000	1.1	1.2	1.3	V
VDD_C	VDD_C LDO output voltage	LDO2_val_register=000		1.2		V
VDD_RF	VDD_RF LDO input / output voltage		1.75	1.9	2.0	V
LDO2_OUT	VDD_ANA LDO output voltage			VDD_RF – 0.12		V
VDD_ANA	Power Pin			1.7		V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VDD_SYNTH	Power Pin			1.7		V
VDD_LNA	VDD_LNA LDO output voltage			VDD_RF – 0.12		V
V_SWITCH_u	Min. voltage on V_RUN to switch from V_BCKP to V_RUN supply			1.26		V
V_SWITCH_l	Min. voltage on V_RUN to switch from V_RUN to V_BCKP supply			1.23		V
POR_B_u	Rising Threshold value for VDD_B			1.18		V
POR_B_l	Falling Threshold value for VDD_B			1.08		V
POR_C_u	Rising Threshold value for VDD_C			1.18		V
POR_C_l	Falling Threshold value for VDD_C			1.08		V
POR_IO	Threshold value for VDD_IO	00 – 1.65 V 01 – 1.8 V 10 – 2.7 V 11 – 3.0 V		1.51 1.63 2.48 2.72		V
POR_MR_u	Rising Threshold value for V_Reset	V_TH open V_TH = 0V		1.65 2.45		V
POR_MR_l	Falling Threshold value for V_Reset	V_TH open V_TH = 0V		1.60 2.35		V

Table 26: Power management unit

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Ileak	Leakage current input pins			< 1		nA
Vil	Low level input voltage		0		0.2*VDD_IO	V
Vih	High level input voltage		0.7*VDD_IO		VDD_IO	V
Vol	Low level output voltage	Iol=4mA			0.4	V
Voh	High level output voltage	Ioh=4mA	VDD_IO - 0.4V			V
Rpu_iic	Pull-up resistor for PIO0…3			13		kΩ
Rpu	Pull-up resistor			115		kΩ
Rpd	Pull-down resistor			87		kΩ

Table 27: Digital IO pins

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Ileak	Leakage current input pins				1	uA
Vil	Low level input voltage	VDD_USB >= 3.0 V	0		0.8	V
Vih	High level input voltage	VDD_USB >= 3.0 V	2.0		VDD_USB	V
Vol	Low level output voltage	R_L = 1.425 kΩ to VDD_USB, VDD_USB >= 3.0 V, 22 Ω external series resistor			0.3	V
Voh	High level output voltage	R_L = 14.25 kΩ to GND, VDD_USB >= 3.0, 22 Ω external series resistor	2.8			V
Rpui	Pull-up resistor, Idle State		900	1200	1575	Ω
Rpuo	Pull-up resistor, Operational State		1425	1925	3090	Ω

Table 28: USB pins

7.2.2 BB AC parameters

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_clk_diff	CLK_P, CLK_N Differential signal amplitude		100			mVpp
RTC_Fxtal	RTC Crystal Resonant Frequency			32768		Hz

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
RTC_T_start	RTC Startup time			1		sec
RTC_Iosc	32KHz OSC current source			1		uA
RTC_Drive	32KHz OSC Drive level	ESR = 50 kΩ		50		nW
RTC_Amp	32KHz OSC oscillation amplitude	ESR = 50 kΩ		141		mVpp
RTC_ESR	32KHz Xtal Equivalent Series Resistance			50		kΩ
RTC_CL	RTC Load capacitance on Crystal	ESR = 50 kΩ	-20%	10.7	+20%	pF

Table 29: Baseband AC parameters

7.2.3 RF AC parameters

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Fin	Receiver Input Frequency			1575.42		MHz
NFtot	Receiver Chain Noise Figure	including 1.6dB SAW-Filter Insertion Loss between LNAOUT and MIX_IN		2.5		dB
RF_NF	Receiver Chain Noise Figure without internal LNA	50 Ohm Referred		9		dB
LNA_S11	LNA Input Return Loss	50 Ohm Environment		-13		dB
LNA_S22	LNA Output Return Loss	50 Ohm Environment		-15		dB
LNA_S21	LNA Power Gain	50 Ohm Environment		16.5		dB
LNA_NF	LNA Noise Figure	50 Ohm Environment		1.9		dB
LNA_IIP3	LNA IIP3 @880 MHz @1710 MHz @1920 MHz	50 Ohm Environment		 2 -8 -1		dBm
RFA_S11	RF Amp Input Return Loss	100 Ohm Differential Input		-15		dB
RF_Min_Gain	Down-conversion Chain Minimum Voltage Gain (LNA excluded)	100 Ohm Differential Input, 10kOhm//1pF Load at PGA output		47.5		dB
RF_Max_Gain	Down-conversion Chain Maximum Voltage Gain (LNA excluded)	100 Ohm Differential Input, 10kOhm//1pF Load at PGA output		91.5		dB
RF_Gain_Step	Down-conversion Chain Voltage-Gain Step	100 Ohm Differential Input, 10kOhm//1pF Load at PGA output		1.5		dB
RF_IIP3	Down-conversion Chain IIP3 @880 MHz @1710 MHz @1920 MHz	100 Ohm Differential Input, 10kOhm//1pF Load at PGA output		 -25 -25 -25		dBm
RF_IQ_CM	RF_I , RF_Q output common-mode voltage	10kOhm // 1pF Load		600		mV
RF_Out_1dB	Down-conversion Chain Output 1dB Compression Point	@3 MHz IF, 10kOhm//1pF Load at PGA output		1.2		V_{pp}
RF_CLK_CM	CLK output common-mode voltage	10kOhm // 1pF Load		600		mV
RF_CLK_DIFF	CLK output differential voltage	@26 MHz, 10kOhm // 1pF Load		500		mV_{pp}
Synth_Lock_Time	Synthesizer Frequency Lock time			500		µs
TCXO_Freq	TCXO Frequency		16.8	26	38.4	MHz
TCXO_IN_VPP	TCXO Input Peak-to-peak Voltage		0.8			V_{pp}
Xtal_Freq	XTO Frequency		26		26	MHz
XTAL_Drive_Level	XTAL Drive Level	@26 MHz, 15 Ohm < ESR < 60 Ohm	12	40	60	uW

Table 30: RF AC parameters

7.2.4 Power consumption

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_BCKP	V_BCKP Backup current	HW Backup mode VDD_B=1.2V, VDD_C=0V, V_RUN=0V		22		uA
I_RUN	V_RUN Backup current	SW Backup mode VDD_B=1.2V, VDD_C = 0V, V_RUN=3V		25		uA
I_SLEEP	V_DCDC Sleep Core current	Sleep mode, VDD_C = 1.2V		400		uA
I_RF_S	VDD_RF Sleep RF current	Sleep mode, VDD_RF =1.8V		0.1		uA
I_RF_T	VDD_RF Tracking RF current	Tracking, VDD_RF =1.8V		20		mA
IDDIO_B	VDD_IO Backup current	Backup mode, VDD_IO=3.3V, VDD_C = 0V, all I/O open		2		uA
IDDIO_S	VDD_IO Sleep current	Sleep mode, VDD_IO =3.3V, VDD_C = 1.2 V, all I/O open		13		uA

Table 31: Power Consumption

☞ All values in Table 31 are measured at 25◦C ambient temperature.

7.3 Indicative power requirements

Table 32 lists examples of the total system supply current including RF and base-band part for a possible application.

☞ Values in Table 32 are provided for customer information only as an example of typical power requirements. Values are characterized on samples, actual power requirements can vary depending on FW version used, external circuitry, number of SVs tracked, signal strength, type of start as well as time, duration and conditions of test.

Parameter		Min	Typ	Max	Unit
Peak supply current				67	mA
Sustained core current[12]	Acquisition		47		mA
	Tracking (Max Performance Mode)[13]		39		mA
	Tracking (Eco Mode)[13]		37		mA
	Tracking (Power Save Mode)[13]		17		mA
Full system backup current[14]	HW backup current		22		uA

Table 32: Indicative power requirements

For more information about power requirements, see the *UBX-G6010, UBX-G6000/UBX-G0010 Hardware Integration Manual* [1].

[12] Use this figure to determine required battery capacity.
[13] FW 6.02, with strong signals, all orbits available. For cold starts typical 12 min after First Fix. For hot starts typical 15 sec after First Fix. Power Save Mode at 1 fix/s.
[14] Dependant on configuration pin settings; configuration pin set to GND draws additional current due to internal pull-ups.

7.4 EMI timing diagrams

The EMI registers are configured with 1 clock cycles CS2_N setup time with respect to WE_N, 1 wait cycle and 1 cycle CS2_N hold time with respect to WE_N. This configuration permits the utilization of standard external memories up to 70 ns read access time classification.

Figure 8 and Figure 9 show respectively the timings for a write and a read access.

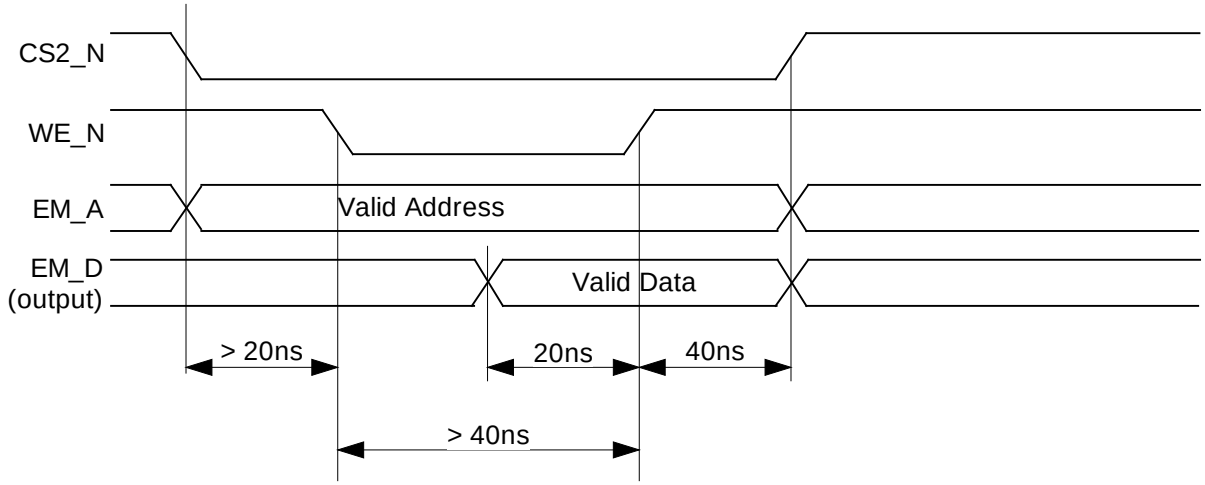


Figure 8: EMI 16-bit write cycle

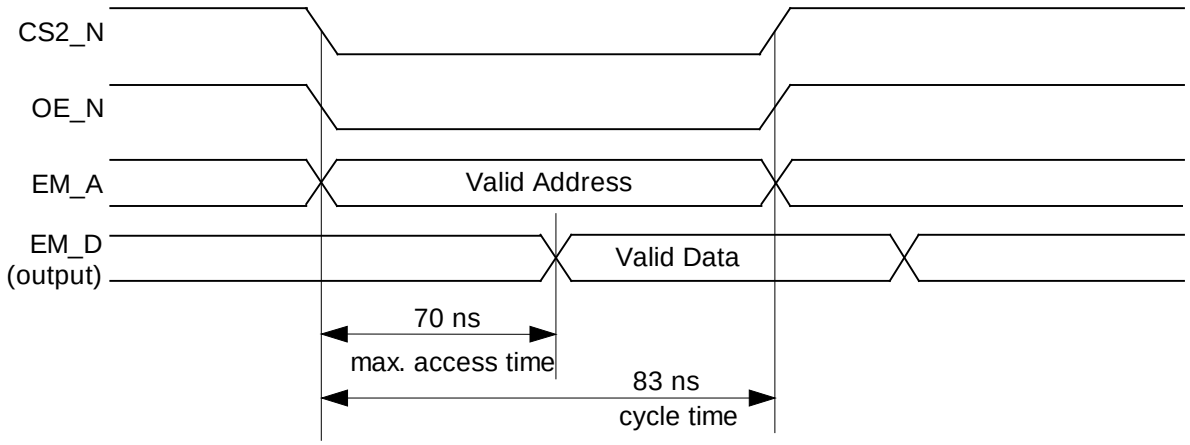


Figure 9: EMI 16-bit read cycle

7.5 SPI timing diagrams

For error free data transmission over SPI interface in slave mode, the timing conditions listed in Table 34 apply. The following signals are relevant for timing constraints:

Symbol	Description
SS_N	Slave Select signal
SCK	Slave Clock signal

Table 33: Symbol description

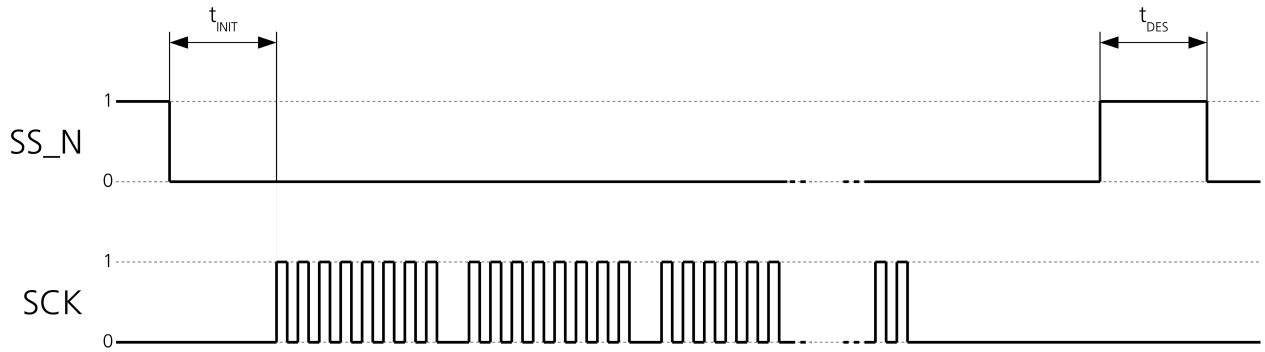


Figure 10: SPI timing diagram

Parameter	Description	Recommendation
t_{INIT}	Initialization Time	500 µs
t_{DES}	Deselect Time	1 ms.
Maximum Bit Rate ROM FW		100 kbit/s
Maximum Bit Rate FLASH FW		50 kbit/s

Table 34: SPI timing recommendations

☞ The values in the above table guarantee error-free transmission. By allowing just a few transmission errors, the bit rate could be increased considerably. These timings – and therefore the bit rate – could also be improved by disabling other interfaces, e.g. UART. When the real-time GPS engine is not used, or when in Capture & Process boot mode, a higher bit rate is possible.

☞ As shown in the above table, the maximum bit rate depends on whether the firmware is running from internal ROM or external FLASH memory.

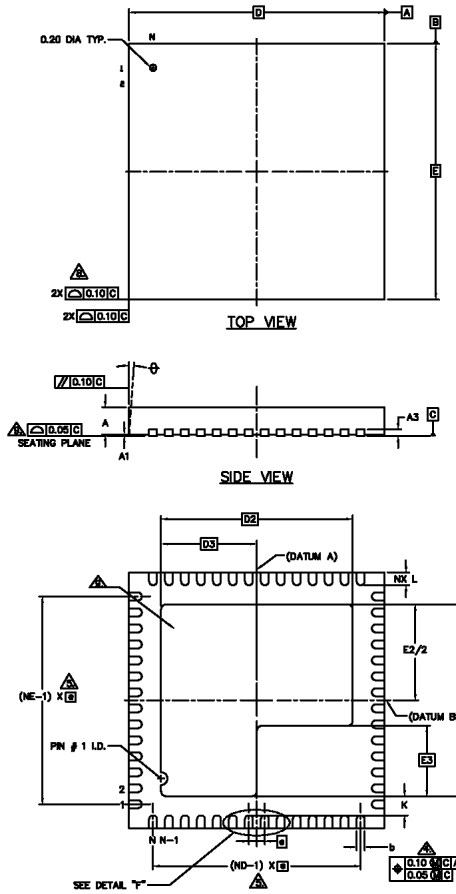
7.6 DDC timing diagrams

The DDC interface is I²C Standard Mode compliant. For timing parameters consult the I²C standard.

☞ The maximum bit rate in slave mode is 100kbit/s. The maximum SCL clock frequency is 100 kHz.

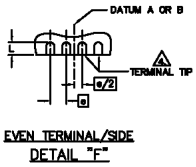
8 Mechanical specification

8.1 MLF56 / UBX-G6010-S



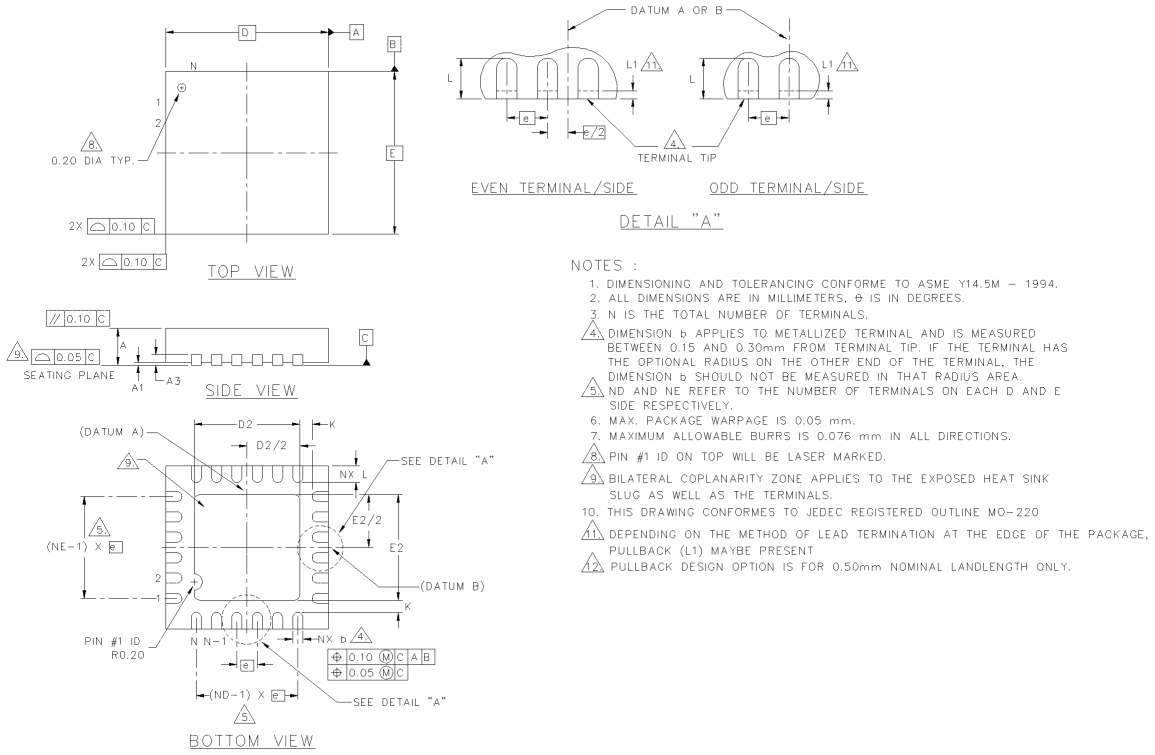
NOTES :

1. DIMENSIONING AND TOLERANCING CONFORME TO ASME Y14.5M – 1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS, θ IS IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
5. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
6. MAX. PACKAGE WARPAGE IS 0.05 mm.
7. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
8. PIN #1 ID ON TOP WILL BE LASER MARKED.
9. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.



Symbol	Min.	Typ.	Max	Note
[e]		0.50 BSC.		
N		56		
ND		14		
NE		14		
L	0.35	0.4	0.45	
b	0.18	0.25	0.30	
D2	5.90	6.00	6.10	
D3	2.90	3.00	3.10	
E2	5.90	6.00	6.10	
E3	2.10	2.20	2.30	
A	0.80	0.85	0.90	
A1	0.00	0.02	0.05	
Θ	0	-	12	2
K		0.20 MIN.		
D		8.0 BSC		
E		8.0 BSC		

8.2 MLF24 / UBX-G0010-Q

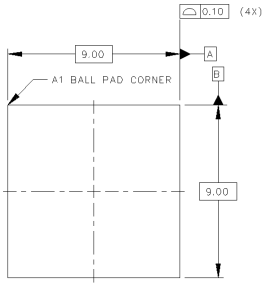


NOTES :

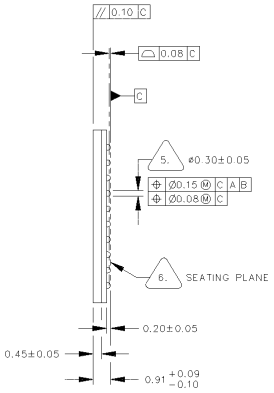
1. DIMENSIONING AND TOLERANCING CONFORME TO ASME Y14.5M – 1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. θ IS IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
5. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
6. MAX. PACKAGE WARPAGE IS 0.05 mm.
7. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
8. PIN #1 ID ON TOP WILL BE LASER MARKED.
9. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
10. THIS DRAWING CONFORMES TO JEDEC REGISTERED OUTLINE MO-220
11. DEPENDING ON THE METHOD OF LEAD TERMINATION AT THE EDGE OF THE PACKAGE, PULLBACK (L1) MAYBE PRESENT
12. PULLBACK DESIGN OPTION IS FOR 0.50mm NOMINAL LANDLENGTH ONLY.

Symbol	Min.	Typ.	Max	Note
[e]		0.50 BSC.		
N		24		
ND		6		
NE		6		
L	0.35	0.4	0.45	
b	0.18	0.25	0.30	
D2	2.50	2.60	2.70	
E2	2.50	2.60	2.70	
A	0.80	0.85	0.90	
A1	0.00	0.02	0.05	
A3		0.20 REF.		
Θ	0	-	12	2
K		0.20 MIN.		
D		4.0 BSC		
E		4.0 BSC		
L1		0.15 mm MAX		11

8.3 CVBGA100 / UBX-G6000-B



TOP VIEW



SIDE VIEW

7. REFERENCE SPECIFICATIONS:
A. AAWW SPEC #001-0531-2234: PACKING OPERATION PROCEDURE.
B. AAWW SPEC #001-0519-2062: MARKING.

6. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

5. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.

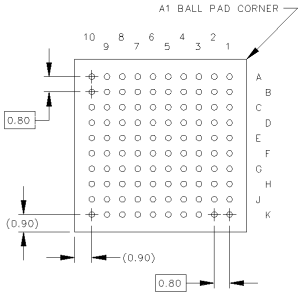
4. THE MAXIMUM ALLOWABLE NUMBER OF SOLDER BALLS IS 100.

3. THE MAXIMUM SOLDER BALL MATRIX SIZE IS 10 X 10.

2. THE BASIC SOLDER BALL GRID PITCH IS 0.80mm.

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994.

NOTES: UNLESS OTHERWISE SPECIFIED



BOTTOM VIEW
100 SOLDER BALLS

9 Reliability tests and approvals

9.1 Reliability tests

Qualifications requirements according to AEC-Q100 "*Failure Mechanism Based Stress Test Qualification For Integrated Circuits*" and appropriate JEDEC standards.

9.2 Approvals

Products marked with this lead-free symbol on the product label comply with the "Directive 2002/95/EC of the European Parliament and the Council on the Restriction of Use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

All u-blox 6 GPS ICs are RoHS compliant and green (no halogens).

10 Product handling

10.1 Packaging

UBX-G6010, UBX-G6000/UBX-G0010 are delivered as reeled tapes in order to enable efficient production, production lot set-up and tear-down.

Figure 11: Reeled u-blox ICs

10.1.1 Reels

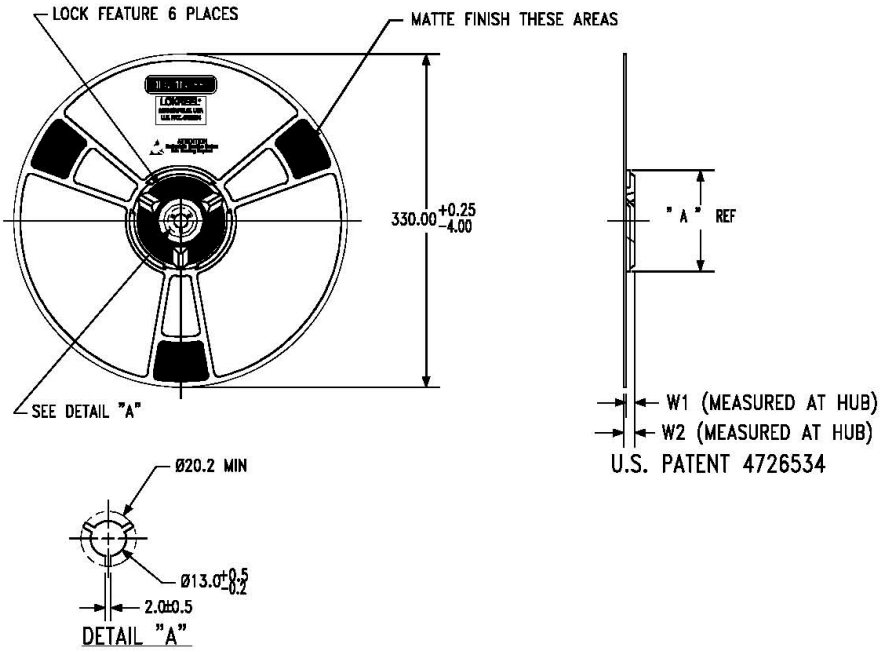
u-blox 6 ICs are deliverable in the following quantities:

- 100 pin CVBGA: 2000 pieces/reel
- 56 pin MLF: 2000 pieces/reel
- 24 pin MLF: 4000 pieces/reel

The dimension of the reel is shown in *Figure 12*.

☞ Hint: Sample quantities are delivered in trays:

- 10 pieces/tray for prototypes
- 100 pieces/tray for pre-production

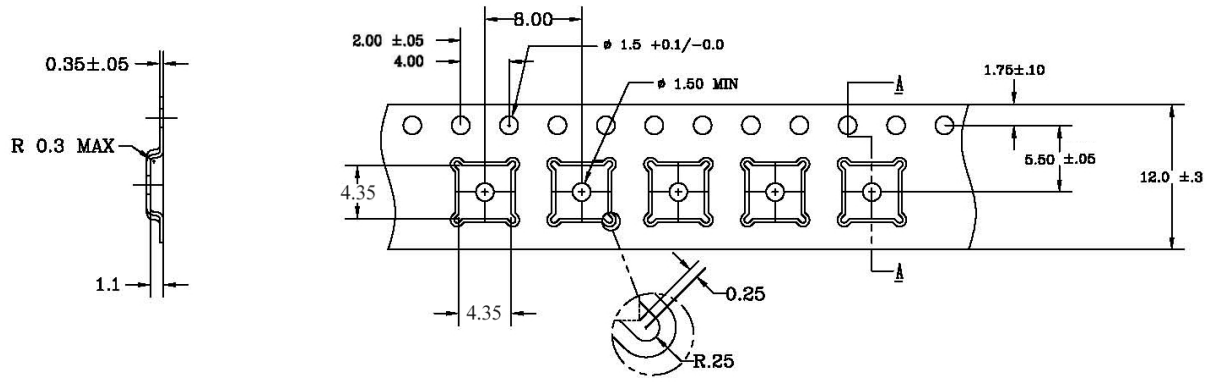


NOMINAL HUB DEPTH	W1	W2 MAX	A	
			mm	inch
4.0	4.4	7.1	102.0	4
4.0	4.4	7.1	102.0	4
28.0	28.4	31.1	102.0	4
8.0	8.4	11.1	102.0	4
8.0	8.4	11.1	101.6	4
16.0	16.4	19.1	101.6	4
16.0	16.4	19.1	101.6	4

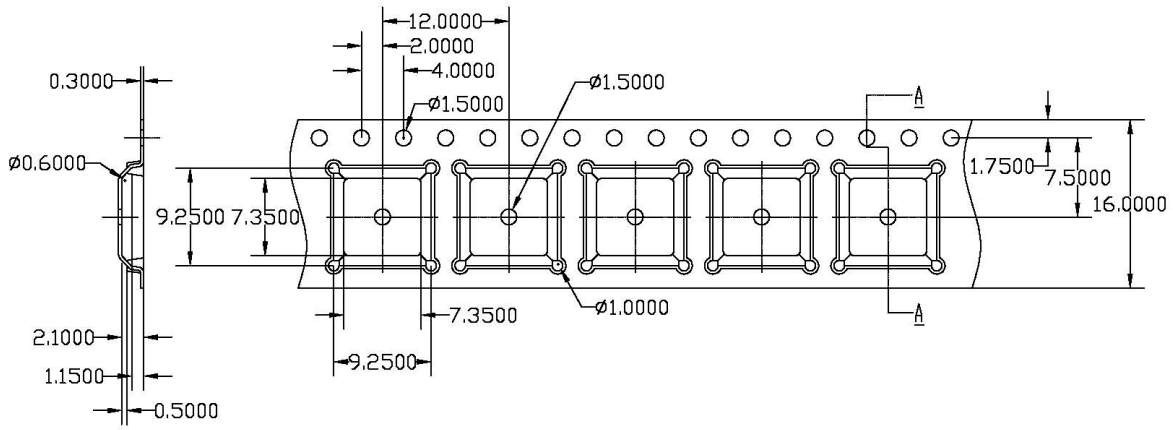
Figure 12: Dimensions of reel

10.1.2 Tapes

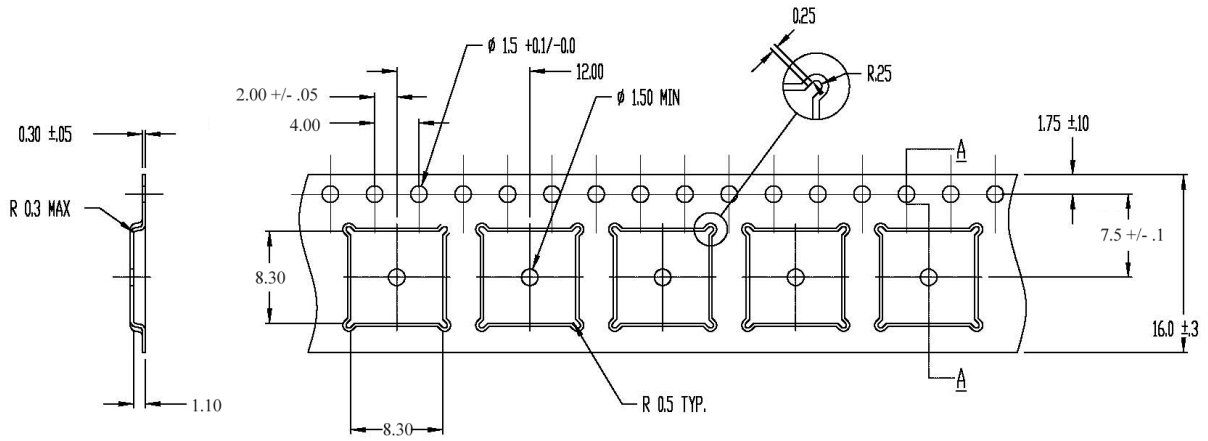
The dimensions of the tapes for u-blox 6 ICs are specified in Figure 13.



Dimensions for QFN24 on tape



Dimensions for CVBGA on tape



Dimensions for QFN56 on tape

Figure 13: Dimensions for u-blox 6 ICs on tape

10.2 Shipment, storage and handling

u-blox 6 ICs are designed and packaged to be processed in an automatic assembly line, and are shipped in Tape-and-Reel.

Some u-blox 6 ICs are Moisture Sensitive Devices (MSD) in accordance to the IPC/JEDEC specification. Appropriate MSD handling instructions and precautions are summarized in Sections 10.2.1 to 10.2.3. Read them carefully to prevent permanent damage due to moisture intake.

GPS receivers contain highly sensitive electronic circuitry and are Electrostatic Sensitive Devices (ESD). Handling u-blox 6 ICs without proper ESD protection may destroy or damage them permanently. See Section 10.2.6 for ESD handling instructions.

10.2.1 Moisture sensitivity levels

The Moisture Sensitivity Level (MSL) relates to the packaging and handling precautions required. Table 35 lists the MSL levels of u-blox 6 ICs.

IC	MSL Level
24 pin MLF	1
56 pin MLF	1
100 pin CVBGA	3

Table 35: MSL levels

For MSL standard see IPC/JEDEC J-STD-020, which can be downloaded from www.jedec.org.

10.2.2 Shipment

Table 36 summarizes the dry pack requirements for different MSL levels in the IPC/JDEC specification.

MSL Level	Dry Pack Requirement
1	Optional
2	Required
2a	Required
3	Required
4	Required

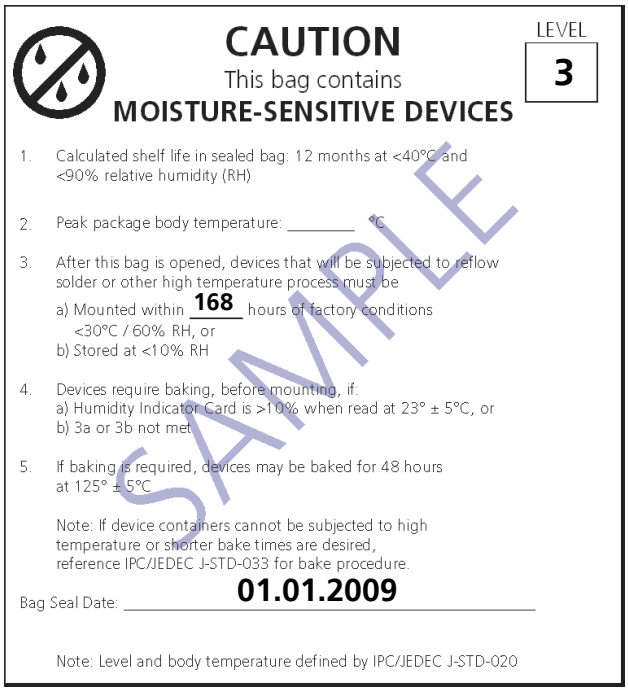
Table 36: JEDEC specification of dry pack requirements

According to IPC/JEDEC specification J-STD-020, if a device passes MSL level 1, it is classified as not moisture sensitive and does not require dry pack. If a device fails level 1 but passes a higher numerical level, it is classified as moisture sensitive and must be dry packed in accordance with J-STD-033.

MSD sensitive u-blox 6 ICs are delivered on Tape-and-Reels in a hermetically sealed package ("dry bag") to prevent moisture intake and protect against electrostatic discharge. For protection from physical damage, the reels are individually packed in cartons.

Carrier materials such as trays, tubes, reels, etc., that are placed in the Moisture Barrier Bag (MBB) can affect the moisture level within the MBB. Therefore, the effect of these materials is compensated by adding additional desiccant in the MBB to ensure the shelf life of the SMD packages.

The dry bag provides an IPC/JEDEC compliant MSD label describing the handling requirements to prevent humidity intake. IPC/JEDEC specifications require that MSD sensitive devices be packaged together with a Humidity Indicator Card (HIC) and desiccant to absorb humidity. If no moisture has been absorbed, the three fields in the HIC indicate blue color. Figure 14 shows examples of an MSD label and HIC.



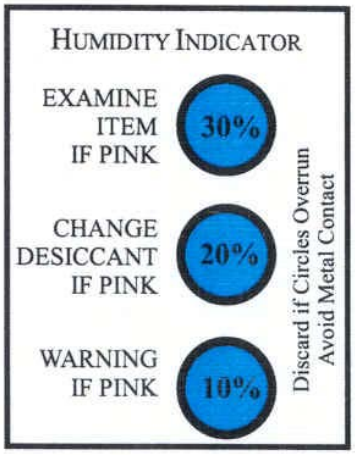


Figure 14: Examples of MSD label and humidity indicator card

10.2.3 Storage and floor life

The calculated shelf life for dry packed SMD packages is a minimum of 12 months from the bag seal date, when stored in a noncondensing atmospheric environment of <40°C/90% RH.

Table 37 lists floor life for different MSL levels in the IPC/JDEC specification.

MSL level	Floor life (out of bag) at factory ambient ≤30°C/60% RH or as stated
1	Unlimited at ≤30°C/85% RH
2	1 year
2a	4 weeks
3	168 hours
4	72 hours

Table 37: JEDEC specification of floor life

The parts must be processed and soldered within the time specified for the MSL level. If this time is exceeded, or the humidity indicator card in the sealed package indicates that they have been exposed to moisture, the devices need to be pre-baked before the reflow solder process.

10.2.4 Drying

Both encapsulant and substrate materials absorb moisture. IPC/JEDEC specification J-STD-020 must be observed to prevent cracking and delamination associated with the "popcorn" effect during reflow soldering. The popcorn effect can be described as miniature explosions of evaporating moisture. Baking before processing is required in the following cases:

- Humidity indicator card: At least one circular indicator is no longer blue
- Floor life or environmental requirements after opening the seal have been exceeded, e.g. exposure to excessive seasonal humidity.

Refer to Section 4 of IPC/JEDEC J-STD-033 for recommended baking procedures. Table 4-1 of the specification lists the required bake times and conditions for drying. For example, a module that has exceeded its floor life by >72 hours shall be baked at 125°C for 9 hours. (Floor life begins counting at time = 0 after bake).

Do not attempt to bake u-blox 6 ICs while contained in tape and rolled up in reels. For baking, place parts individually onto oven tray.

Oxidation Risk: Baking SMD packages may cause oxidation and/or intermetallic growth of the terminations, which if excessive can result in solderability problems during board assembly. The temperature and time for baking SMD packages are therefore limited by solderability considerations. The cumulative bake time at a temperature greater than 90°C and up to 125°C shall not exceed 96 hours. If the bake temperature is not greater than 90°C, there is no limit on bake time. Bake temperatures higher than 125°C are not allowed.

10.2.5 Reflow soldering

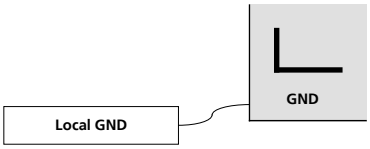
Reflow profiles are to be selected according to IPC/JEDEC J-STD-020.

10.2.6 ESD handling precautions

u-blox 6 receivers are Electrostatic Sensitive Devices (ESD). Observe precautions for handling! Failure to observe these precautions can result in severe damage to the GPS receiver!

GPS receiver ICs are sensitive to ESD and require special precautions when handling. Particular care must be used when handling patch antennas, due to the risk of electrostatic charges. In addition to standard ESD safety practices, the following measures should be taken into account whenever handling the receiver.

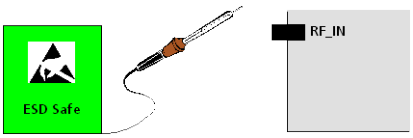
- Unless there is a galvanic coupling between the local GND (i.e. the work table) and the PCB GND, then the first point of contact when handling the PCB shall always be between the local GND and PCB GND.



- When handling the RF-IC or placing components connected to the RF inputs or outputs, do not come into contact with any charged capacitors and be careful when contacting materials that can develop charges (e.g. patch antenna ~10pF, coax cable ~50-80pF/m, soldering iron, …)

- To prevent electrostatic discharge through the RF input, do not touch any exposed antenna area. If there is any risk that such exposed antenna area is touched in non ESD protected work area, implement proper ESD protection measures in the design.

- When soldering components, make sure to use an ESD safe soldering iron (tip).



11 Default settings

Interface	Settings
Serial Port 1 Output	9600 Baud, 8 bits, no parity bit, 1 stop bit Configured to transmit both NMEA and UBX protocols, but only following NMEA and no UBX messages have been activated at start-up: **GGA, GLL, GSA, GSV, RMC, VTG, TXT**
USB Output	Configured to transmit both NMEA and UBX protocols, but only following NMEA and no UBX messages have been activated at start-up: **GGA, GLL, GSA, GSV, RMC, VTG, TXT** USB Power Mode: Bus Powered
Serial Port 1 Input	9600 Baud, 8 bits, no parity bit, 1 stop bit, Autobauding disabled Automatically accepts following protocols without need of explicit configuration: UBX, NMEA The GPS receiver supports interleaved UBX and NMEA messages.
USB Input	Automatically accepts following protocols without need of explicit configuration: UBX, NMEA The GPS receiver supports interleaved UBX and NMEA messages. USB Power Mode: Bus Powered
TIMEPULSE (1Hz Nav)	1 pulse per second, synchronized at rising edge, pulse length 100ms
Power Mode	Maximum Performance Mode

Table 38: Available protocols.

☞ Please refer to the *u-blox 5 & u-blox 6 Receiver Description Including Protocol Specification* [2] for information about further settings.

12 Labeling and ordering information

12.1 Product labeling

12.1.1 BGA100, MLF56

BGA100 and MLF56 semiconductor products provide 4 lines of text:

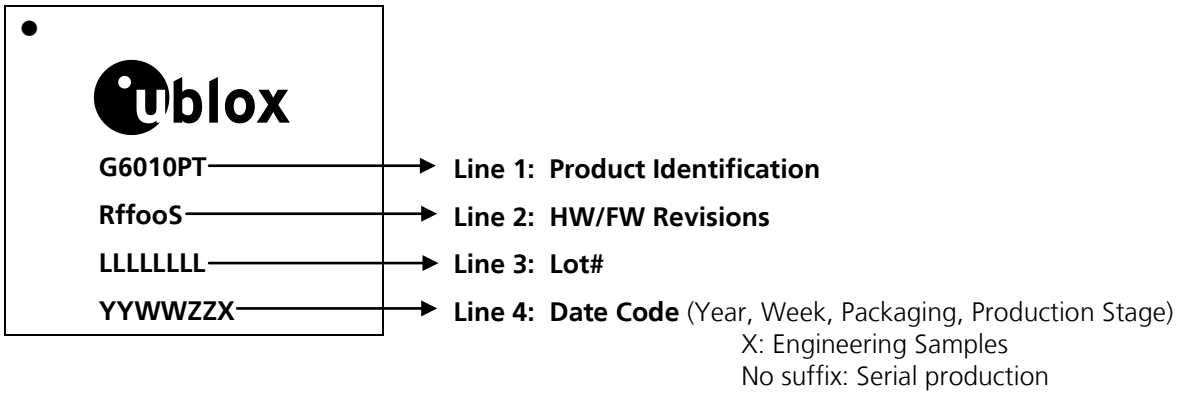


Figure 15: Description of BGA100/MLF56 product label

12.1.2 MLF24

The top surface of the RF front End IC does not provide sufficient space for printing all required contents. The product identification and other information is provided in a compressed format, fitting on 3 rows of text with maximum 6 characters.

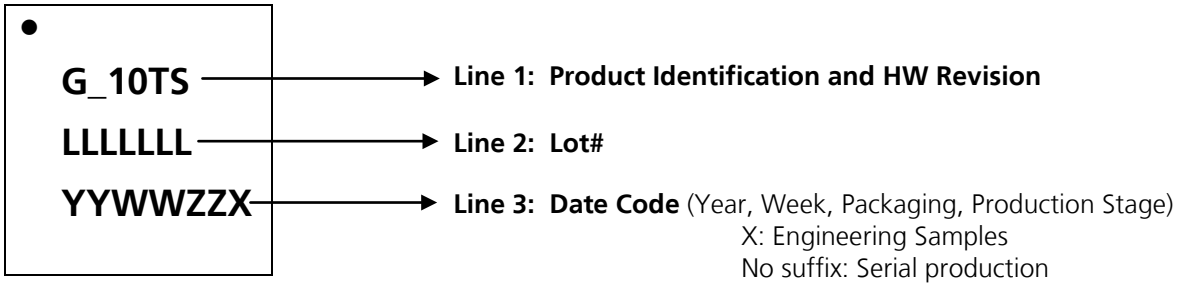


Figure 16: Description of MLF24 product label

12.2 Explanation of product codes

3 different product code formats are used. The **Product Name** is used in documentation such as this datasheet and identifies all u-blox 6 products, independent of packaging and quality grade. The **Ordering Code** includes packaging and quality, while the **Type Number** includes the hardware and firmware versions. Table 39 below details these 3 different formats:

Format	Structure
Product Name	UBX-Gmmnn
Ordering Code	UBX-Gmmnn-PT
Type Number	UBX-Gmmnn-PTRffoo S

Table 39: Product code formats

The parts of the product code are explained in Table 40.

Code	Meaning	Example
UBX	u-blox	
G	GNSS Product	
mm	Baseband core	00 = No core 60 = u-blox 6 BB core
nn	RF core	00 = No core 10 = u-blox 6 RF core
P	Package Type	S = MLF 56 Q = MLF 24 B = CVBGA 100
T	Quality grade	T = Mobile Terminal, Telecom A = Automotive
R	Baseband Hardware Revision	Increasing Alphabetic Character
ff	Firmware Revision	Increasing Number
oo	OTP revision	Increasing Number
S	RF Hardware Revision	Increasing Alphabetic Character

Table 40: part identification code

12.3 Ordering codes

Ordering No.	Product
Standard Type	
UBX-G6010-ST	u-blox 6 Single Package GPS Receiver, 56 Pin MLF(QFN)
Automotive Type	
UBX-G6010-SA	u-blox 6 Single Package GPS Receiver, 56 Pin MLF(QFN)
UBX-G6000-BA	u-blox 6 Baseband Processor, 100 pin CVBGA
UBX-G0010-QA	u-blox RF Front-End IC, 24 pin MLF(QFN)

Table 41: Product ordering codes

☞ Product changes affecting form, fit or function are documented by u-blox. For a list of Product Change Notifications (PCNs) see our website at: http://www.u-blox.com/customersupport/pcn/ublox5IC.html.

Related documents

[1] UBX-G6010, UBX-G6000/UBX-G0010 Hardware Integration Manual, Docu. No. GPS.G5-X-07015

[2] u-blox 5 & u-blox 6 Receiver Description Including Protocol Specification, Docu. No. GPS-X-07036

[3] u-blox 5 LNA Design Application Note, Docu. No. GPS.G5-RF-07043

[4] Power Management Considerations Application Note, Docu. No. GPS.G5-CS-08022

☞ For regular updates to u-blox documentation and to receive product change notifications please register on our homepage.

For complete contact information visit us at www.u-blox.com

Revision history

Revision	Date	Name	Status / Comments
-	5/15/2009	tgri	Initial release
A	2/04/2010	athi	Status "Advanced Information"
B	7/07/2010	athi	Status "Preliminary"
B1	8/07/2010	athi	Clean-up of SPI & DDC speed specifications in sections 2.2.3, 2.2.4, 7.5, and 7.6
B2	22/07/2010	athi	Correction of MLF56 package dimensions (E2/D2 in section 8.1)

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